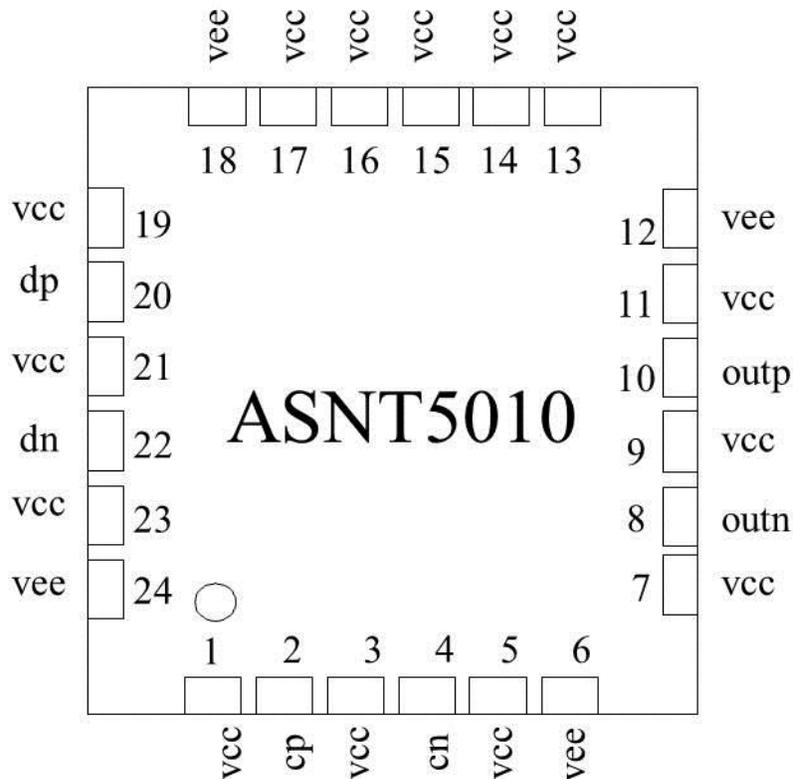




ASNT5010-PQC DC-17Gbps D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 8ps set-up/hold time capability
- 89% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 415mW
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



DESCRIPTION

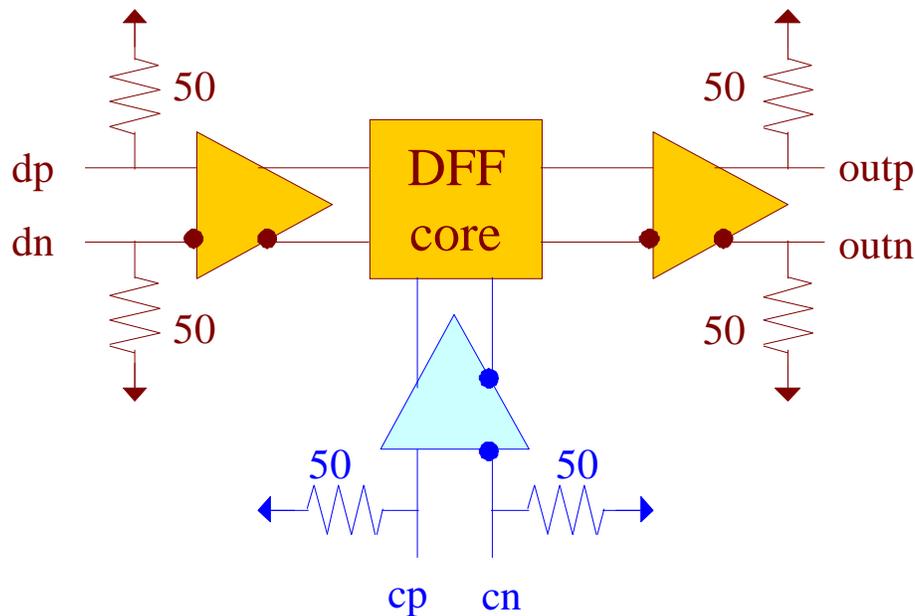


Fig. 1. Functional Block Diagram

The temperature stable ASNT5010-PQC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal dp/dn with a full-rate external clock cp/cn to create a full-rate retimed NRZ data output outp/outn.

The part's I/O's support the CML logic interface with on chip 50 Ω termination to VCC and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (VCC = 0.0V = ground and VEE = -3.3V), or positive supply (VCC = +3.3V and VEE = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50 Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.



All the characteristics detailed below assume $v_{cc} = 0.0V$ and $v_{ee} = -3.3V$.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (v_{ee})		-3.6	V
Power Consumption		0.46	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
dp	20	CML input	Differential data inputs with internal SE 50 Ω termination to v_{cc}
dn	22		
cp	2	CML input	Differential clock inputs with internal SE 50 Ω termination to v_{cc}
cp	4		
outp	10	CML output	Differential data outputs with internal SE 50 Ω termination to v_{cc} . Require external SE 50 Ω termination to v_{cc}
outn	8		
Supply and Termination Voltages			
Name	Description		Pin Number
v_{cc}	Positive power supply (+3.3V or 0)		1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 19, 21, 23
v_{ee}	Negative power supply (0V or -3.3V)		6, 12, 18, 24



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
v _{ee}	-3.1	-3.3	-3.5	V	±6%
v _{cc}		0.0		V	External ground
I _{vee}		125		mA	
Power consumption		415		mW	
Junction temperature	-40	25	125	°C	
HS Input Data (dp/dn)					
Frequency	DC		17	Gbps	
Swing	0.05		0.8	V	Differential or SE, p-p
CM Voltage Level	v _{cc} -0.8		v _{cc}	V	Must match for both inputs
Setup/Hold time		8		ps	
HS Input Clock (cp/cn)					
Frequency	DC		17	GHz	
Swing	0.05		0.8	V	Differential or SE, p-p
CM Voltage Level	v _{cc} -0.8		v _{cc}	V	Must match for both inputs
Clock Phase Margin	85	87	89	%	
HS Output Data (outp/outn)					
Data rate	DC		17	Gbps	
Latency		67		ps	From Clock input to Data output
Logic "1" level		v _{cc}		V	
Logic "0" level		v _{cc} -0.4		V	With external 50Ωm DC termination
Clock-to-output delay	55	65	75	ps	
Rise/Fall times			20	ps	20%-80%
Output Jitter			10	ps	Peak-to-peak

PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the v_{ee} plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5010-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

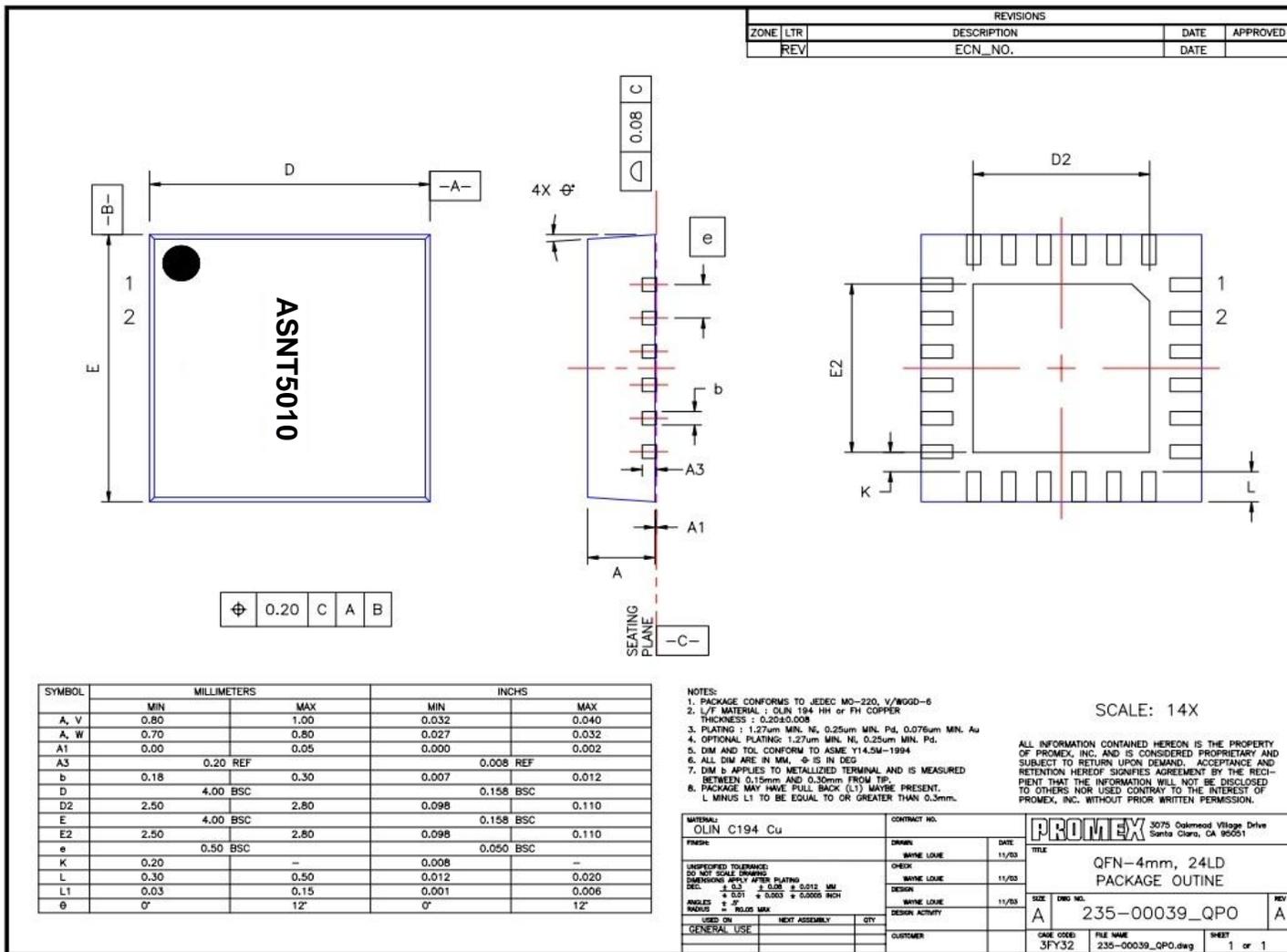


Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)



REVISION HISTORY

Revision	Date	Changes
3.6.2	02-2020	Updated Package Information
3.5.2	07-2019	Updated Letterhead
3.5.1	02-2019	Added setup/hold time to Electrical Characteristics table
3.4.1	08-2018	Corrected latency specifications
3.3.1	08-2018	Added latency specifications
3.2.1	06-2018	Updated electrical characteristics
3.1.1	02-2013	Revised title Revised package information
3.0.1	01-2013	Added package pin out drawing Revised functional block diagram Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Added package information and mechanical drawing Format correction
2.0	07-2009	Revised electrical characteristics
1.0	02-2008	First release