X9470

RF Power Amplifier (PA) Bias Controller

FN8204
Rev 0.00
March 8, 2005

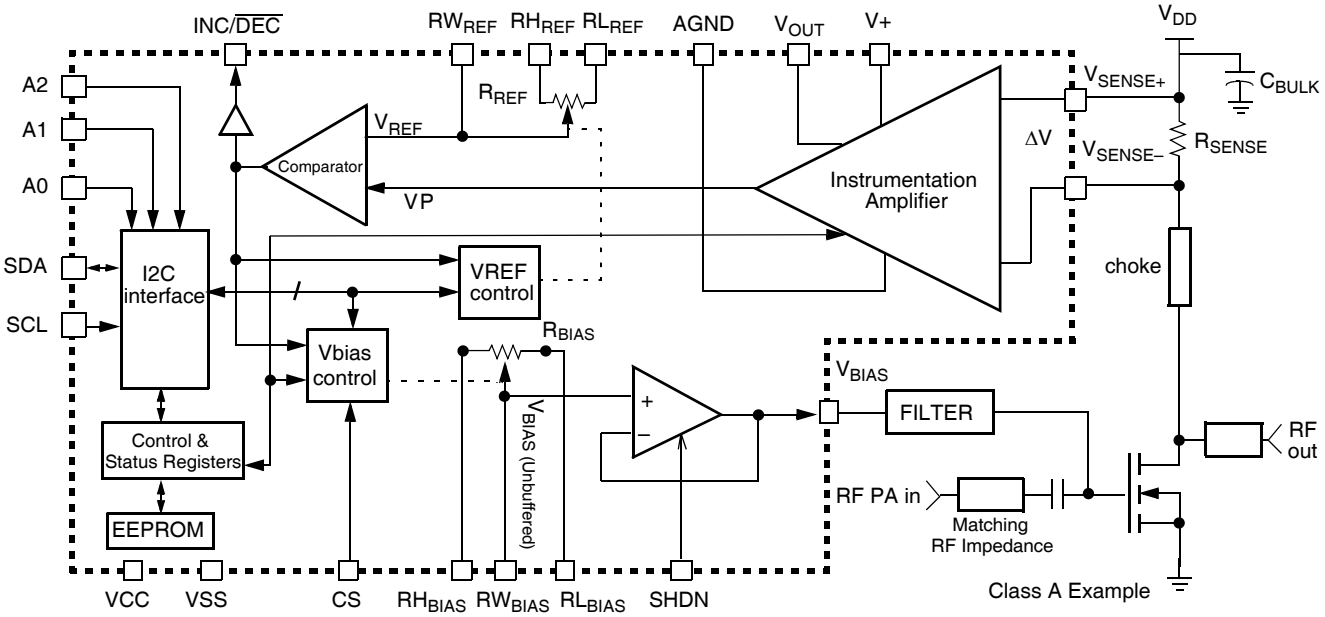
FEATURES

- **Programmable Bias Controller IC for Class A and AB LDMOS Power Amplifiers**
- **Adaptive System on Chip Solution**
- **Bias Current Calibration to better than ±4% using Reference Trim DCP**
- **Automatic Bias Point Tracking and Calibration**
  - **— I_{DQ} Sensing and Tracking**
  - **—Programmable Instrumentation Amplifier to Scale Wide Range of I_{DQ}**
  - **—Programmable Gate Bias Driver**
  - **—All Programmable settings are Nonvolatile**
  - **—All Settings Recalled at Power-up.**
- **28V Maximum V_{DD}**
- **2 Wire Interface for Programming Bias Setting and Optimizing I_{DQ} Set Point**
- **Bias Level Comparator**
- **Shutdown Control pin for PA Signal**
- **Slave address to allow for multiple devices**
- **24-pin TSSOP Package**
- **Applications: Cellular Base Stations (GSM, UMTS, CDMA, EDGE), TDD applications, Point-to-multipoint, and other RF power transmission systems**

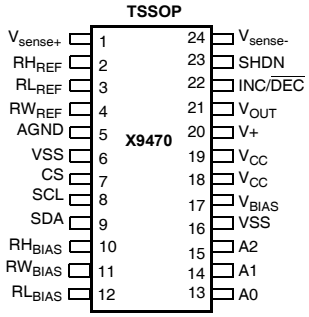
DESCRIPTION

The Intersil X9470 RF PA Bias Controller contains all of the necessary analog components to sense the PA drain current through an external sense resistor and automatically control the gate bias voltage of an LDMOS PA. The external sense resistor voltage is amplified by an instrumentation amplifier and the output of the amplifier along with an external reference voltage is fed to the inputs of a comparator. The comparator output indicates which direction the LDMOS gate bias voltage will move in the next calibration cycle. System calibration is accomplished by enabling the X9470 and providing a clock to the SCL pin. The LDMOS drain current can be maintained constant over temperature and aging changes by periodic calibration. The VOUT pin can be used to monitor the average power by tracking the drain current. Up to eight X9470 or additional Intersil Digital Potentiometers can be controlled via a two-wire serial bus.

TYPICAL APPLICATION



PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Temperature Range	Package
X9470V24I	-40°C TO 85°C	24-Lead TSSOP

PIN DESCRIPTIONS

TSSOP pin	Symbol	Brief Description
1	V_{SENSE+}	Positive sense voltage input terminal
2	RH_{REF}	Upper Terminal of Potentiometer, called the R_{REF} potentiometer. The voltage applied to this pin will determine the upper voltage limit of the adjustment for the Up/Down threshold of the comparator.
3	RL_{REF}	Lower Terminal of Potentiometer, called the R_{REF} potentiometer. The voltage applied to this pin will determine the lower voltage limit of the adjustment for the Up/Down threshold of the comparator.
4	RW_{REF}	Wiper Terminal of Potentiometer, called the R_{REF} potentiometer. The voltage on this pin will be the threshold for the Up/Down comparator. Also referred to as the V_{REF} of the comparator.
5	AGND	Analog ground to allow single point grounding external to the package to minimize digital noise.
6	VSS	System (Digital) Ground Reference
7	CS	Chip Select. This input enables bias calibration adjustments to the R_{BIAS} potentiometer. CMOS input with internal pull-down.
8	SCL	Dual function. Function 1: The increment control input. Increments or decrements the RBIAS potentiometer. Function 2: Serial Data Clock Input. Requires external pull-up.
9	SDA	Serial Data Input. Bi-directional 2-wire interface. Requires external pull-up.
10	RH_{BIAS}	Upper Terminal of Potentiometer, called the R_{BIAS} potentiometer. The voltage applied to this pin will determine the upper limit of the bias voltage to the PA (or V_{BIAS} pin).
11	RW_{BIAS}	Wiper Terminal of Potentiometer, called the R_{BIAS} potentiometer. This voltage is the equivalent to the unbuffered voltage that will appear at the V_{BIAS} pin.
12	RL_{BIAS}	Lower Terminal of Potentiometer, called the R_{BIAS} potentiometer. The voltage applied to this pin will determine the lower limit of the bias voltage to the PA (or V_{BIAS} pin).
13	A0	External address pin which allows for a hardware slave address selection of this device. This pin has an internal pull-down.
14	A1	External address pin which allows for a hardware slave address selection of this device. This pin has an internal pull-down.
15	A2	External address pin which allows for a hardware slave address selection of this device. This pin has an internal pull-down.
16	VSS	System (Digital) Ground Reference
17	V_{BIAS}	This is the bias output voltage pin and is used to drive the filter network to the PA gate.
18	V_{CC}	System (Digital) Supply Voltage
19	V_{CC}	System (Digital) Supply Voltage
20	V +	Positive voltage supply for the instrumentation amplifier and other analog circuits.
21	V_{OUT}	Instrumentation Amplifier output that is 20x or 50x the voltage across the Rsense pins.
22	INC/$\overline{DEC}$	Status output that indicates the state of the comparator. When this pin is HIGH, the RBIAS potentiometer will increment; when the pin is LOW, the RBIAS potentiometer will decrement. This pin is open drain and requires external resistor pull-up.
23	SHDN	Shutdown the output op amp. When SHDN is active (HIGH), the V_{BIAS} pin is pulled LOW.
24	V_{SENSE-}	Negative sense voltage Input terminal

ABSOLUTE MAXIMUM RATINGS*

Voltage on V+ (referenced to AGND) 7V
Voltage on VCC (reference to VSS) 7V
Voltage on all RH, RW, RL pins
(reference to AGND): 7V
Voltage on Vsense+ or
Vsense- (reference to AGRND)..... 30V
Voltage on SDA, CS, SCL, SHDN
(reference to AGND) ..... -0.3V to (Vcc + 0.3V)
Current into Output Pin:..... ±5mA
Continuous Power Dissipation: 500mW
Operating Temperature range:..... -40°C to +85°C
Junction Temperature: ..... 150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds): ..... 300°C

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
INSTRUMENTATION AMPLIFIER

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
V_{IN}(10)	Common Mode Input Voltage on V_{SENSE+} and V_{SENSE-} pins	20		28	V	
Gain 1	Gain from V_{SENSE} to V_{OUT}(2)		20		V/V	Measured with Status Register bit SR0 = 0
Gain 2	Gain from V_{SENSE} to V_{OUT}(2)		50		V/V	Measured with Status Register bit SR0 = 1
V_{RANGE1}	Differential voltage sense range between V_{SENSE+} and V_{SENSE-} for gain 1		60	90	mV	Gain = 20
V_{RANGE2}	Differential voltage sense range between V_{SENSE+} and V_{SENSE-} for gain 2		40	60	mV	Gain = 50
V_{OS}	Input Offset Voltage		0.5		mV	V_{SENSE} = 40mV to 90mV T_A = 25°C
Av1	Gain 1 Error Gain = 20 (4)		1.5		%	V_{SENSE} = 60mV to 90mV T_A = 25 to 85°C, Gain = 20
Av2	Gain 2 Error Gain = 50 (4)		1.5		%	V_{SENSE} = 40mV to 60mV T_A = 25 to 85°C, Gain = 50
Avt1	Total Error, Gain 1 Gain = 20 (5)	-6	1.5	6	%	V_{SENSE} = 60mV to 90mV T_A = 85°C, Gain = 20
			10		%	V_{SENSE} = 60mV to 90mV T_A = 25 to 85°C, Gain = 20
Avt2	Total Error, Gain 2 Gain = 50 (5)	-6	1.5	6	%	V_{SENSE} = 40mV to 60mV T_A = 85°C, Gain = 50
			10		%	V_{SENSE} = 40mV to 60mV T_A = 25 to 85°C, Gain = 50
At	Long Term Drift		2		%	Avt1 or Avt2
SR(10)	Slew Rate of Instrumentation Amp		0.2		V/µS	ΔV_{SENSE} = 20mV step, Cout = 10pF Measured at V_{OUT}(1,3)

ELECTRICAL CHARACTERISTICS

INSTRUMENTATION AMPLIFIER (CONTINUED)

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
T_{settle}(10)	Setting time of Instrumentation Amp		5.0		µS	ΔV_{SENSE} = 20mV step, Cout = 10pF, settling to 1% of final value Measured at V_{OUT}(1,3)
CMRR	Common Mode Rejection Ratio		40		dB	For both Gain 1 and Gain 2
PSRR	Power Supply Rejection Ratio		55		dB	For both Gain 1 and Gain 2
V_{OUT} Range	V_{OUT} Voltage Swing	0.3		1.8	V	Gain = 20
		0.3		3.0	V	Gain = 50
V_{OUT} Noise(10)	V_{OUT} Voltage Noise, rms		3		mV	Gain = 20
I_{VSENSE}(10)	V_{SENSE+}, V_{SENSE-} Input Bias Current		250		µA	T_A = 25°C
C_{VSENSE}(10)	V_{SENSE+}, V_{SENSE-} Input Capacitance		10		pF	Each Input

COMPARATOR

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
VOL	Output Voltage Low on the INC/$\overline{DEC}$ pin			0.4	V	IOL = 1mA
Io(10)	Output sink Current			3	mA	INC/$\overline{DEC}$ pin, open drain
Vos(10)	Input Hysteresis		20		mV	Vcc = 5 V
Tpd(10)	Response Time for propagation delay		2		µS	INC/$\overline{DEC}$ pin with 2kΩ pull up

VREF DCP CIRCUIT BLOCK

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
R_{TOTAL}	End to End Resistance	8	10	12	kΩ	
	Number Taps or Positions			64		
V_{RH}	RH_{REF} Terminal Voltage	AGND		V_+	V	AGND = 0V
V_{RL}	RL_{REF} Terminal Voltage	AGND		V_+	V	AGND = 0V
V_{RW}	RW_{REF} Terminal Voltage	AGND		V_+	V	AGND = 0V
	Power Rating(10)		2.5		mW	R_{TOTAL} =10kΩ
	Resolution(10)		1.6		%	
	Absolute Linearity(6)	-0.2		+0.2	MI(8)	
	Relative Linearity(7)	-0.2		+0.2	MI(8)	

VREF DCP CIRCUIT BLOCK

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
	R_{TOTAL} Temperature Coefficient(10)		±300		ppm/°C	
	Ratiometric Temperature Coefficient(10)	-20		+20	ppm/°C	
C_{IN}(10)	Potentiometer Capacitances on RH_{REF} and RL_{REF}		10		pF	

BIAS ADJUSTMENT DCP CIRCUIT BLOCK

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
R_{TOTAL}	End to End Resistance Variation	8	10	12	kΩ	with ±20% variation
	Number Taps or Positions			256		
V_{RH}	Voltage at the RH_{BIAS} Terminal Voltage	AGND		V_+	V	AGND = 0V
V_{RL}	Voltage at the RL_{BIAS} Terminal Voltage	AGND		V_+	V	AGND = 0V
V_{RW}	Voltage at the RW_{BIAS} Terminal Voltage	AGND		V_+	V	AGND = 0V
	Power Rating(10)		2.5		mW	R_{TOTAL} =10 KΩ
	Resolution(10)		0.4		%	
	Absolute Linearity(6)	-1.0		+1.0	MI(8)	
	Relative Linearity(7)	-1.0		+1.0	MI(8)	
	R_{TOTAL} Temperature Coefficient(10)		±300		ppm/°C	
	Ratiometric Temperature Coefficient(10)	-50		50	ppm/°C	
C_{IN}(10)	Potentiometer Capacitances on RH_{BIAS} and RL_{BIAS}		10		pF	

VBIAS OUTPUT VOLTAGE FOLLOWER

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
V_{OS}	Input Offset Voltage		10		mV	
$V_{OSDRIFT}$(10)	Offset Voltage Temperature Coefficient		10		µV/°C	T_A = -40 to +85°C
SR	Output Slew Rate on V_{BIAS}		0.5		V/µS	R_L = 10kΩ, 1nF, ΔV_{BIAS} = 20mV
V_{BIAS}	Voltage Output Swing	1.5		V_{CC} - 0.5	V	I_{OUT} = ±10mA
T_S(10)	Settling Time		2		µs	Final value ±1%, R_L = 10kΩ, 1nF, ΔV_{BIAS} = 20mV
t_{SHDN}	Time for SHDN pin (delay) valid		0.1	1.0	µs	
PSRR	Power Supply Rejection Ratio	45	55		dB	VCC supply V_{CC} = 4.75 to 5.25V

VBIAS OUTPUT VOLTAGE FOLLOWER

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
	Input Voltage Range	1.5		V_{CC} - 0.5	V	
C_L(10)	Load Capacitance		1		nF	
C_{IN}(10)	Capacitances on Shutdown Pin		10		pF	
R_{OUT}(10)	Output Impedance		3		Ω	at 5MHz, 1nF load

D.C. OPERATING CHARACTERISTICS

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}(9)	V+ Active Current		1	3	mA	CS = V_{CC} - 0.3V, and SCL @ max. $t_{CYC, SDA}$ = V_{CC} - 0.3V, SHDN inactive
I_{CC2}(9)(10)	V_{CC} Active Current		5	25	mA	
I_{SB}(9)	Standby Supply Current (V_{CC}, V+)		1.5		mA	CS = V_{IL}, and SCL inactive (no clock), $_{SDA}$ = V_{IL}, SHDN active
I_{LI}	CS, SDA, SCL, SHDN RH, RL, RW, INC/$\overline{DEC}$ VOUT, Input Leakage	-10		10	µA	V_{IN} = VSS to V_{CC}
V_{IH}(10)	CS, SDA, SCL, SHDN, A0, A1, A2 HIGH Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}(10)	CS, SDA, SCL, SHDN, A0, A1, A2 LOW Voltage	-0.5		V_{CC} x 0.3	V	
C_{IN}(10)	CS, SDA, SCL, SHDN, A0, A1, A2 Capacitance		10		pF	V_{CC} = 5V, V_{IN} = VSS, T_A = 25°C, f = 1MHz

Notes: (1) V_{OUT} is a high impedance output intended for light loads only.
(2) Gain at V_{OUT} is set to 20 by default.
(3) Value given is for V_{OUT}. The V_{BIAS} output will depend on the V_{BIAS} potentiometer which is initially loaded with a zero value, then followed by the loading of the final value from E^2 memory.
(4) Gain Error excludes the contribution of the input offset voltage error.
(5) Total Error includes the contributions of gain error and input offset voltage error.
(6) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{w(n)}$(actual) - $V_{w(n)}$(expected))
(7) Relative Linearity is a measure of the error in step size between taps = $V_{W(n+1)}$ - [$V_{w(n)}$ + MI]
(8) 1 MI = Minimum Increment = R_{TOT}/63 or R_{TOT}/255.
(9) Typical values are for T_A = 25°C and nominal supply voltage, VCC = 5V.
(10) This parameter is not 100% tested.

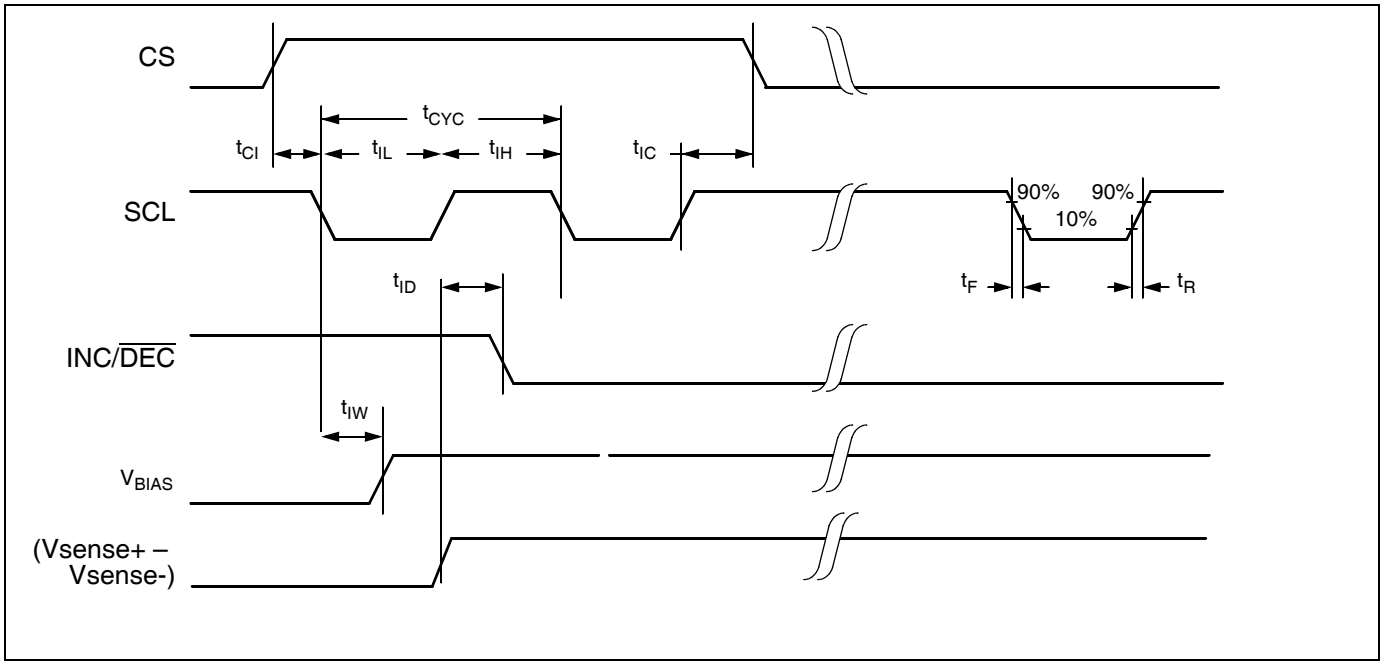
BIAS ADJUSTMENT CIRCUIT BLOCK

A.C. OPERATING CHARACTERISTICS

Recommended Operating Conditions: (Vcc, V+ = 4.75 to 5.25V; Vsense+, Vsense- = 26V; T_A = -40°C to +85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Units
		Min.	Typ.(9)	Max.	
t_{CI}	CS to SCL Setup	100			ns
t_{ID}	Vsense Change to INC/$\overline{DEC}$ Change		5		µs
t_{IL}	SCL LOW Period	1.5			µs
t_{IH}	SCL HIGH Period	1.5			µs
t_{IC}(10)	SCL Inactive to CS Inactive	100			ns
t_{IW}(10)(11)	SCL to V_{BIAS} Change		3		µs
t_{CYC}	SCL Cycle Time	3			µs
t_R, t_F(10)	SCL Input Rise and Fall Time			500	ns

A.C. TIMING



Note: (11) MI in the A.C. timing diagram refers to the minimum incremental change in the V_{BIAS} output due to a change in the wiper position.

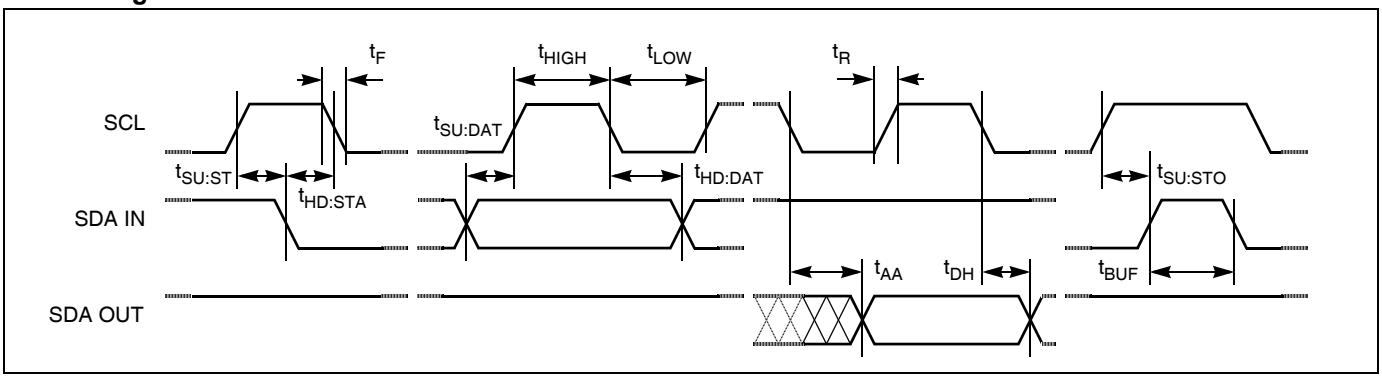
AC SPECIFICATIONS

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
t_{IN}(10)	Pulse width Suppression Time at inputs	50		ns
t_{AA}(10)	SCL LOW to SDA Data Out Valid	0.1	0.9	µs
t_{BUF}(10)	Time the bus must be free before a new transmission can start	1.3		µs
t_{LOW}	Clock LOW Time	1.3		µs
t_{HIGH}	Clock HIGH Time	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	0.6		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
$t_{SU:DAT}$	Data In Setup Time	200		ns
$t_{HD:DAT}$	Data In Hold Time	200		ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}(10)	Data Output Hold Time	50		ns
t_R(10)	SDA and SCL Rise Time	20 +.1Cb(12)	300	ns
t_F(10)	SDA and SCL Fall Time	20 +.1Cb(12)	300	ns
Cb(10)	Capacitive load for each bus line		400	pF

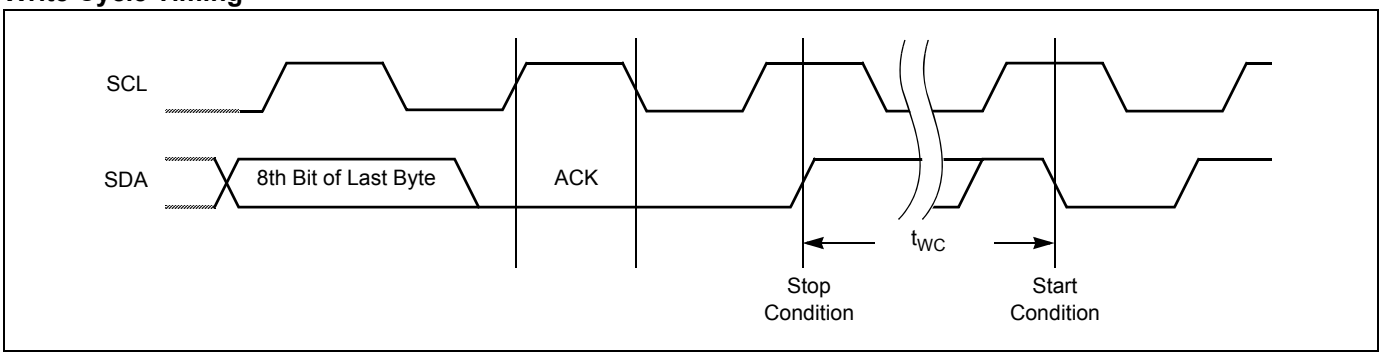
Note: (12) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

Bus Timing



Write Cycle Timing



Power-up Timing

Symbol	Parameter	Min.	Max.	Unit
$t_r V_{CC}$ (10)	V_{CC} Power-up rate	0.2	50	V/ms

Note: Delays are measured from the time V_{CC} is stable until the specified operation can be initiated. These parameters are not 100% tested. Proper recall of stored wiper setting requires a V_{CC} power-up ramp that is monotonic and with noise or glitches < 100mV. It is important to correctly sequence voltages in an LDMOS amplifier circuit. For the X9470 typical application, the V_{CC}, then V+ pins should be powered before the V_{DD} of the LDMOS to prevent LDMOS damage. Under no circumstances should the V_{DD} be applied to the LDMOS device before V_{CC} and V+ are applied to the X9470.

DCP Default Power-up Tap Positions (shipped from factory)

VREF DCP	0
Bias Adjust DCP	0

Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{WC} (10)	Write Cycle Time		5	10	ms

Note: t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

DETAILED PIN DESCRIPTIONS

Supply Pins

Digital Supplies VCC, VSS

The positive power supply and ground for the DCP digital control sections. VSS is normally tied to digital ground. The X9470 is provided with separate digital and analog power supply pins to better isolate digital noise from the analog section.

Analog Supplies V+, AGND

The positive analog supply and ground for the Instrumentation Amplifier (IA). The analog supply ground is kept separate to allow an external single point connection. V+ can be a separate supply voltage from VCC, or VCC can be filtered before connection to V+.

Bias Adjustment Circuit Block Pins

RH_{BIAS} , RL_{BIAS} , and RW_{BIAS} for VBIAS Adjustments.

These pins are the connections to a Intersil Digitally Controlled Potentiometer (XDCP™) or R_{BIAS} potentiometer. RH_{BIAS} is connected to the most positive reference, and the RL_{BIAS} is connected to the least positive reference voltage. The potentiometer has a resolution of 256-taps and typical R_{TOTAL} of 10kΩ. So for example, to provide 4mV resolution, the voltage difference applied to the RH_{BIAS} and RL_{BIAS} pins must be 1.024V. The RW_{BIAS} value can be stored in non-volatile memory and recalled upon power-up.

Serial Clock (SCL).

This is a dual function input pin. The state of the CS pin determines the functionality.

Function 1: SCL is a negative edge-triggered control pin of the R_{BIAS} potentiometer. Toggling SCL will either increment or decrement the wiper in the direction indicated by the logic level on the INC/$\overline{DEC}$ pin. CS must be high for this function.

Function 2: SCL is the serial bus clock for serial bus interface. CS must be low for this function.

Chip Select (CS). Calibration Enable.

The CS input is the enable bias adjustments. When the CS is HIGH (enabled) and a SCL pulse is present, the wiper position on the R_{BIAS} potentiometer will automatically update with either an increment or decrement of one tap position according to INC/$\overline{DEC}$ signal from the comparator.

When CS is LOW (disabled), the wiper counter of the XDCP will hold the last wiper position until CS is enabled again and the wiper position is updated.

INC/$\overline{DEC}$ Monitor Pin

The Up or Down Monitor pin (INC/$\overline{DEC}$) indicates the state of the comparator. This signal indicates that the Instrumentation Amplifier output voltage is higher or lower than the voltage level set by the RW_{REF} pin. The output is used to indicate the direction that the gate bias voltage needs to move to reach the target bias voltage.

Sense and Scale Block Pins

V_{SENSE+} and V_{SENSE-}

These are the input pins to the IA circuit. These pins are used to determine the change in voltage across the the external drain sense resistor of an RF power amplifier.

RH_{REF} , RL_{REF}, and RW_{REF}. PA Bias Set Point.

The PA Bias reference voltage is controlled by a 64-tap (10kΩ typical R_{TOTAL}) potentiometer, called the R_{REF} potentiometer. The voltages applied to RH_{REF} and RL_{REF} will determine the range of adjustment of the reference voltage level (VREF) for the Comparator. The resolution of the comparator reference is the difference of the voltages applied to RH_{REF} and RL_{REF} divided by 63. The position of the wiper (RW_{REF}) is controlled via serial bus. The RW_{REF} value can be stored in non-volatile memory and recalled upon power-up.

RW_{REF} is also an input signal used as a scaling voltage (VREF) to set the appropriate I_{DQ} of an RF power amplifier. V_{REF} can be derived from an external voltage divider or from a baseband processor or similar microcontroller. V_{REF} can be set permanently or changed dynamically using the potentiometer for various PA operating points.

V_{OUT}

This pin is the output of the IA, which reflects a 20x or 50x gain of the input signal (voltage across the Vsense pins). It can be used to indicate the magnitude of the drain current envelope when RF is present.

Output Block Pins

V_{BIAS}

The V_{BIAS} is the gate bias voltage output. It is buffered with a unity gain amplifier and is capable of driving 1nF (typical) capacitive loads.

This pin is intended to be connected through an RF filter to the gate of an LDMOS power transistor. The voltage of V_{BIAS} is determined by the XDCP's value of the R_{BIAS} resistor.

Other Pins

SHDN

SHDN is an input pin that is used to shutdown the V_{BIAS} output voltage follower. When the SHDN pin is HIGH, the V_{BIAS} pin is pulled to VSS. When the device is shutdown, the current R_{BIAS} wiper position will be maintained in the wiper counter register. When shutdown is disabled, the wiper returns to the same wiper position before shutdown was invoked. Note that when the device is taken out of shutdown mode (SHDN goes from HIGH to LOW), the CS input must be cycled once to enable calibration.

SDA

Serial bus data input/output. Bi-directional. External pullup is required.

A0, A1, A2

Serial bus slave address pins. These pins are used to defined a hardware slave address. This will allow up to 8 of the X9470's to be shared on one two-wire bus. These are useful if several X9470's are used to control the bias voltages of several LDMOS Power Transistors in a single application. Default hardware slave address is "000" if left unconnected due to internal pull-down resistor.

TYPICAL APPLICATION

The X9470 can be used along with a microprocessor and transmit control chips to control and coordinate FET biasing (see Figure 1). The CS, SCL, and SDA signals are required to control the X9470 Bias Adjustment Circuit Block. An internal R_{WREF} voltage is provided via a programmable voltage divider between the RH_{REF} and RL_{REF} pins and is used to set the voltage reference of the comparator. The shutdown (SHDN) and bias voltage indicators (INC/$\overline{DEC}$) are additional functions that offer FET control, monitoring, and protection.

Typically, the closed loop setup of the X9470 allows for final calibration of a power amplifier at production test. The CS and SCL pins are used to perform this calibration function. Once in a base station, the amplifier can then be re-calibrated any time that there is no RF signal present. The bias setting block can also be used open loop to adjust gate bias or can be shutdown using the SHDN pin. The sense and scale block can be used for amplifier power monitoring diagnostics as well.

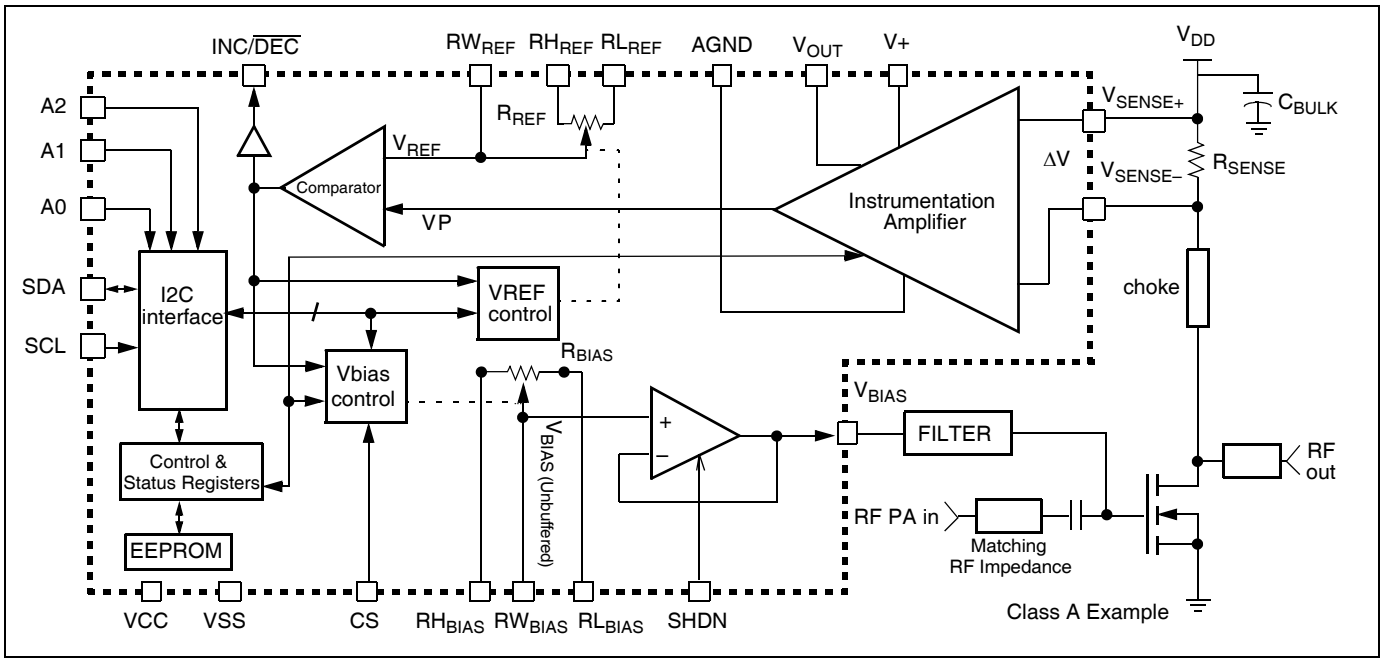
The range of the drain bias current operating point of the LDMOS FET is set by an external reference across the reference potentiometer. The wiper of the potentiometer sets the trip point for comparison with V_P, the amplified voltage across R_{SENSE}, the drain resistor. The output of the comparator causes the R_{BIAS} potentiometer to increment or decrement automatically on the next SCL clock cycle. This R_{BIAS} potentiometer is configured as a voltage divider with a buffered wiper output which drives the gate voltage of an external LDMOS FET.

Once the optimum bias point is reached, the R_{BIAS} value is latched into a wiper counter register. Again, the V_{BIAS} gate voltage can be updated continuously or periodically depending on the system requirements.

Both terminals of the R_{BIAS} potentiometer are access-ible and can be driven by external reference voltages to achieve a desired I_{DQ} vs. gate voltage resolution, as well as supporting temperature compensation circuitry.

In summary, the X9470 provides full flexibility on setting the operating bias point and range of an external RF power amplifier for GSM, EDGE, UMTS, CDMA or other similar applications.

Figure 1. Typical Application



X9470 FUNCTIONAL DESCRIPTION

This section provides detail description of the following:

– Sense and Scale Block Description

– Bias Adjustment Control Block Description

– Output Block Description

– Bias Adjustment and Storage Description

SENSE AND SCALE BLOCK

The Sense and Scale Circuit Block (Figure 2) implements an instrumentation amplifier whose inputs (V_{SENSE+} and V_{SENSE-}) are across an external sense resistor in the drain circuit of an RF Power FET. V_{SENSE+} is connected to V_{DD}, the drain voltage source for the RF power FET, and V_{SENSE-} pin is connected to the other end the external sense resistor.

An internal instrumentation amplifier (IA) will sense the ΔV and amplify it by a gain factor of K_1 (see Equation 1). The resulting output is compared with V_{REF} at the comparator. V_{REF} can be a fixed reference voltage or adjusted by using the 64-tap digital potentiometer. The output of the comparator is used to increment or decrement the R_{BIAS} potentiometer in the Bias Adjustment Circuit Block. The gain factor K_1 is designed such that the Sense and Scale Block will set the Bias Adjustment Circuit Block to operate in a given voltage range (mV) vs. drain current adjustment (mA).

$$I_{DQ} \cong \frac{V_{REF}}{K_1 * R_{SENSE}} \quad (1)$$

K_1 is fixed 50x for the internal comparator input.

The output of the IA is also available at the pin Vout to enable drain current monitoring. The gain at Vout is fixed at a factor of K_2, lower than K_1 so that high I_{DQ} currents will not cause saturation of the Vout signal. The equation for Vout is given as:

$$\Delta V = I_{DQ} * R_{SENSE}$$

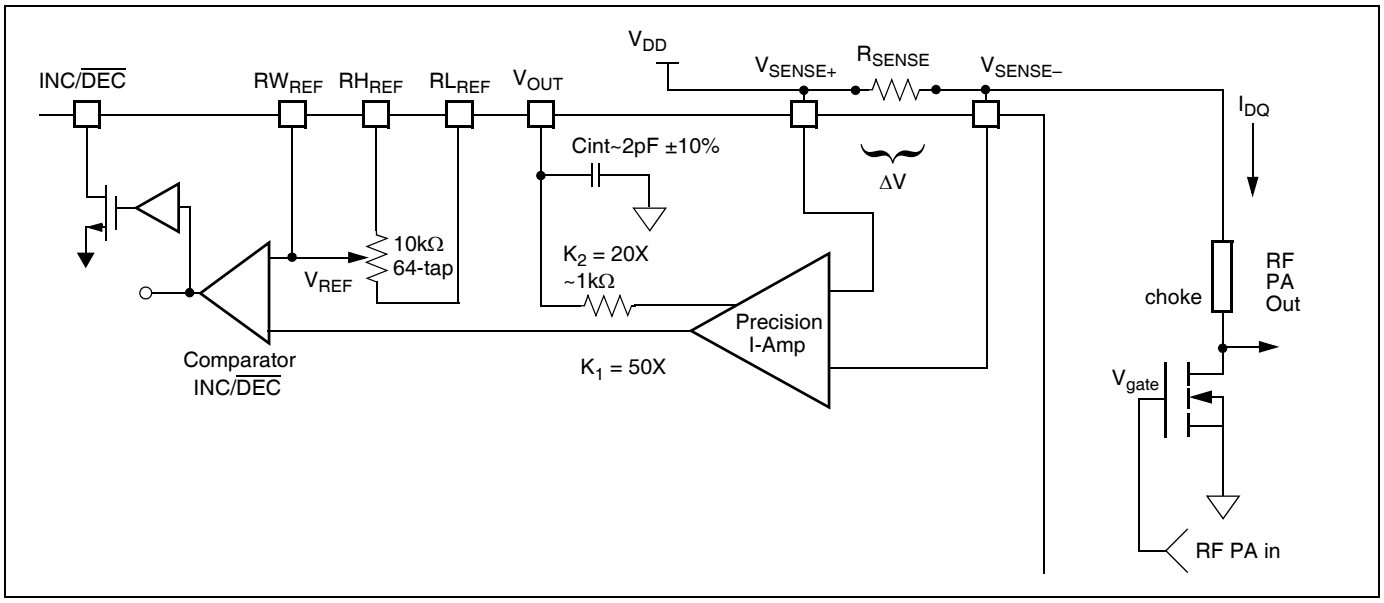
$$V_{OUT} = K_2 * \Delta V$$

K_2 is fixed to 20x for the Vout pin

BIAS ADJUSTMENT CIRCUIT BLOCK

There are three sections of this block (Figure 3): the input control, counter and decode section (1), the resistor array (2); and the non-volatile register (3). The input control section operates just like an up/down counter. The input of the counter is driven from the output of the comparator in the Sense and Scale Block and is clocked by the SCL signal. The output of this counter is decoded to select one of the taps of a 256-tap digital potentiometer.

Figure 2. Sense and Scale Block Diagram



The wiper of the digital potentiometer acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme. The electronic switches in the potentiometer operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} (SCL to RW_{BIAS} change).

When the device is powered-up, the X9470 will load the last saved value from the non-volatile memory into the WCR. Note that the current wiper position can be saved into non-volatile memory register by using the SCL and CS pins as shown in Figure 4.

Important note: the factory setting of the wiper counter register is the ZERO-position (0 of 255 taps). This is the default wiper position.

Bias Adjustment Block Instructions and Programming. The SCL, INC/$\overline{\text{DEC}}$ (internal signal) and CS inputs control the movement of the wiper along the resistor array. (See Table 1) With CS set HIGH, the device is selected and enabled to respond to the INC/$\overline{\text{DEC}}$ and SCL inputs. HIGH to LOW transitions on SCL will increment or decrement R_{BIAS} (depending on the state of the INC/$\overline{\text{DEC}}$ input). The INC/$\overline{\text{DEC}}$ input is derived from the output of the comparator of the Sense and Scale Block.

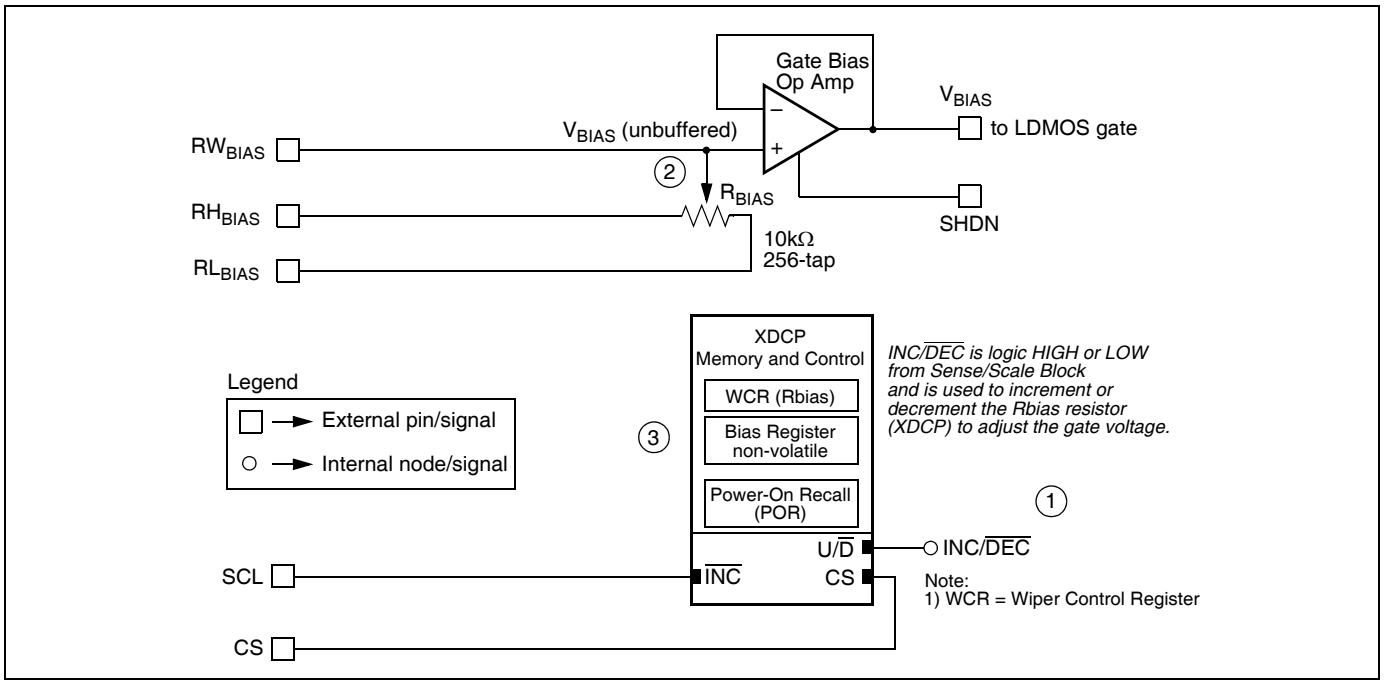
Storing Bias Resistor Values in Memory. Wiper values are stored to VOLATILE memory automatically when CS is HIGH and INC/$\overline{\text{DEC}}$ either transitions from HIGH to LOW or from LOW to HIGH. Wiper values are stored to NON-VOLATILE memory during Byte Write or as described in the following section.

Table 1. Mode Selection

SDA	CS*	$\overline{\text{SCL}}$	INC / DEC	Mode
H	H	↘	H	VBIAS is incremented one tap position.
H	H	↘	L	VBIAS is decremented one tap position.
H	H	X	↘ or ↗	Lock Wiper Position. Save to volatile memory. (BiasLock™)
X	L	X	X	Open Loop.

* When coming out of shutdown, the CS pin must be cycled once before bias adjustment is enabled.

Figure 3. Bias Adjustment Block Diagram



NON-VOLATILE STORE OF THE BIAS POSITION

The following procedure will store the values for the Rref and Rbias wiper positions in Non-Volatile memory. This sequence is intended to be performed after a BiasLock calibration sequence to simplify storage. If BiasLock has not been achieved, then the Rbias wiper position may change when the CS pin is brought high and SCL begins clocking. See Figure 4 for the actual sequence.

1. Set the WEL bit with a write command (02h to register 0Fh)
2. Peform a calibration and achieve BiasLock. Leave CS pin high.
3. Write the address byte only (START, followed by device/slave address and a 0 for a write, see page 19).
4. Perform a STOP command.
5. With SCL still low, bring the CS low. The falling edge of the CS will initiate the NV write.

The WEL bit may be reset afterwards to prevent further NV writes.

INC/$\overline{\text{DEC}}$ FUNCTION

The INC/$\overline{\text{DEC}}$ pin is an open-drain logic output that tracks the activity of the increment/decrement comparator. A logic HIGH at INC/$\overline{\text{DEC}}$ indicates that the I_{DQ} did not rise up to the desired setting indicated by V_{REF} while a logic LOW at the INC/$\overline{\text{DEC}}$ pin indicates that the IDQ is higher than the desired setting.

INC/$\overline{\text{DEC}}$ is used as an internal control signal as well. As an example, when INC/$\overline{\text{DEC}}$ is LOW, the Bias Adjustment Circuit Block will start to move the Rbias resistor wiper towards the RL_{BIAS} terminal end when CS is HIGH and SCL is clocking. Consequently, the V_{BIAS} voltage will decrease, and the I_{DQ} decreases to meet the desired V_{REF} setting.

The INC/$\overline{\text{DEC}}$ signal can also be used to detect a damaged RF power FET. For instance, If INC/$\overline{\text{DEC}}$ stays HIGH during and after a calibration sequence it may indicate that the RF power FET has failed. This indicator can also be used with a level sense on the V_{OUT} pin to perform diagnostics.

SHUTDOWN MECHANISM

This hardware control shutdown pin (SHDN) will pull the voltage of V_{BIAS} to VSS with an internal pull down resistor. When shutdown is disabled (V_{BIAS} is active when SHDN is LOW), the V_{BIAS} voltage will move to the previous desired bias voltage.

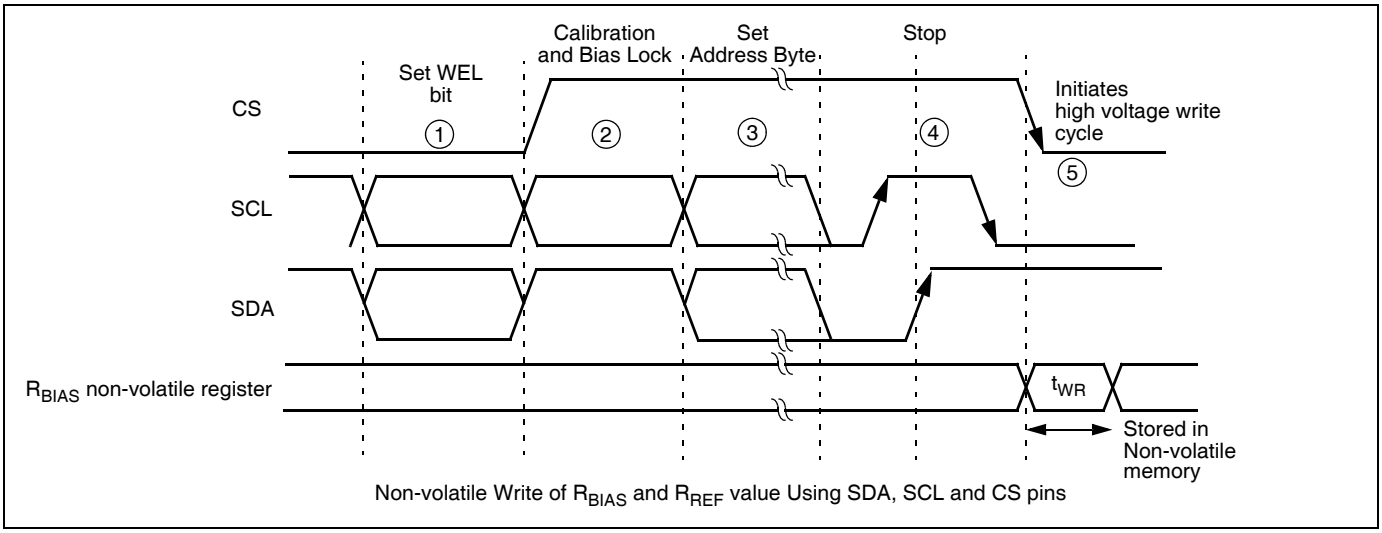
It will take less than a microsecond to enable the internal output buffer depending on the loading condition at the V_{BIAS} pin.

OUTPUT (V_{BIAS})

V_{BIAS} is a buffered output of RW_{BIAS} (wiper output). It can deliver a high current for driving up to typically 1nF capacitive loading with stable performance and fast settling time.

A single pole filter should be placed in between the V_{BIAS} output and the RF input signal to isolate any high frequency noise.

Figure 4. Non-Volatile Store of the Bias Position



X9470 PRINCIPLES OF OPERATION

The X9470 is a Bias Controller that contains all the necessary analog components for closed-loop DC bias control of LDMOS Transistors in RF Applications. The X9470 provides a mechanism to periodically set DC bias operating points of Class A or AB-type amplifiers to account for V_{GS} drift and temperature variations. The following is an example of X9470 operation.

The X9470 incorporates an instrumentation amplifier, comparator and buffer amplifier along with resistor arrays and their associated registers and counters. The serial interface provides direct communication between the host and the X9470. This section provides a detailed example of how the X9470 can be used to calibrate and dynamically set the optimum bias operating point of an RF power amplifier (see Figure 5):

– State 0: Power-on Monitor Mode
– State 1: DC-bias Setting When No RF is Present [Calibration]
– State 2: Calibration Disable When RF is Present
– State 3: PA Standby Mode. Dynamic Adjustment for V_{GS} drift and Temperature variation
– State 4: Power Off (Shutdown) Mode [Turn off the Power Amplifier]

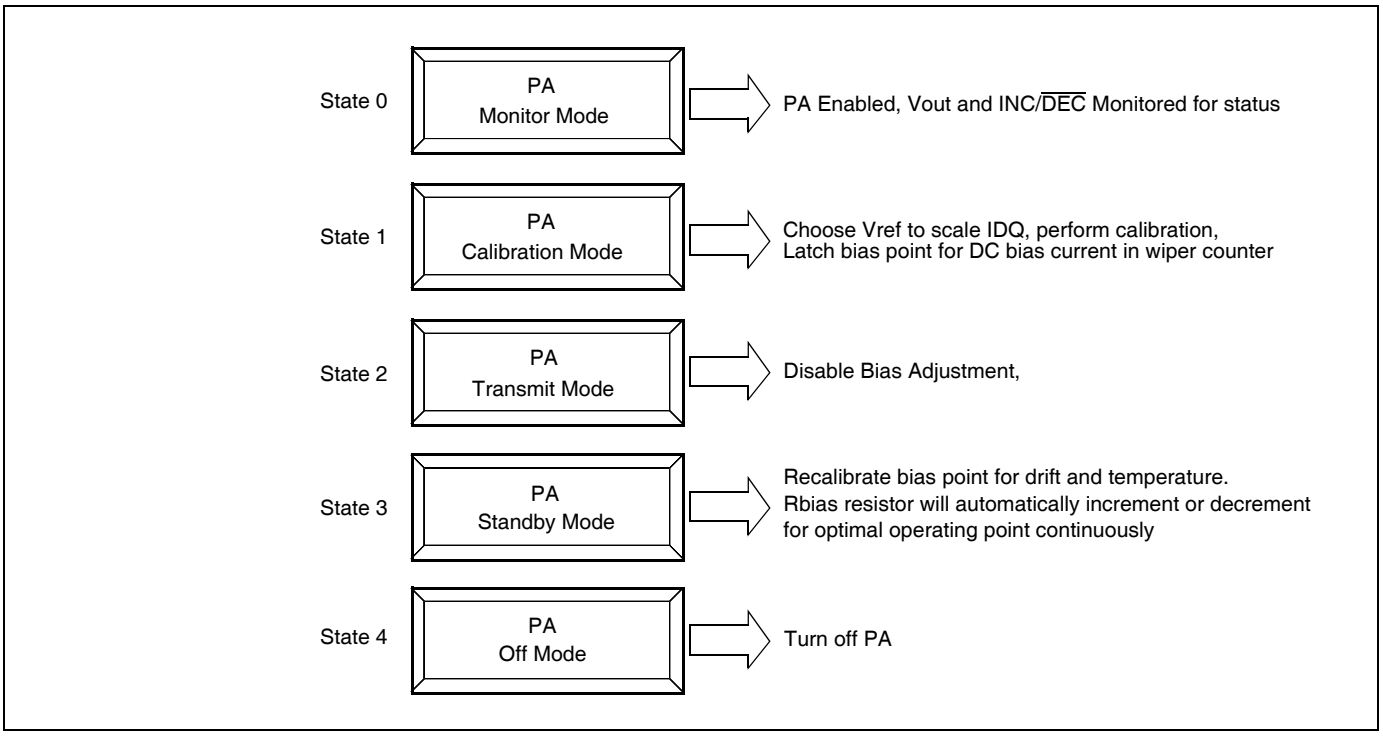
State 0: Monitor Mode

The V_{OUT} and INC/$\overline{DEC}$ outputs of the X9470 can be used for monitoring and diagnostic purposes. Since V_{OUT} has a lower gain (20x, default) than the internal IA output, it can handle higher drain sense current while keeping the output below the rail. This allows normal PA power monitoring, and over-current sensing using an external comparator. The INC/$\overline{DEC}$ pin can be monitored during calibration to see if there is no change, which indicates LDMOS functional problems. Note that the INC/$\overline{DEC}$ status is also available in the status register for software status reads.

State 1: DC-bias Setting When No RF is Present [Calibration]

At calibration, the DC bias operating point of the LDMOS Power Amplifier must be set. As soon as the Bias Adjustment Circuit Block is enabled (CS enabled, SDA high, and SCL pulse provided), the X9470 will automatically calibrate the external Power Amplifier by continually sampling the drain current of the external Power Amplifier and make adjustments to the gate voltage of the amplifier (See Figure 6).

Figure 5. Operating modes X9470



When no RF signal is present, the instrumentation amplifier of the X9470 senses the drain current as a voltage drop, ΔV, across an external drain R_{sense} resistor. The ΔV is amplified and compared to an external scaling voltage, V_{REF}. Any difference between ΔV and V_{REF} results in a resistive increment or decrement of the internal R_{BIAS} potentiometer.

The R_{BIAS} potentiometer is used as a voltage divider with the RH_{BIAS} and RL_{BIAS} terminals setting the upper and lower voltage limits of the unbuffered RW_{BIAS} voltage. The resolution of the R_{BIAS} potentiometer resistor is 0.4% of the difference of voltage across the RH_{BIAS} and RL_{BIAS} terminals. The R_{TOTAL} is typically 10kΩ with 256-taps. So, for example, if the difference between the RH_{BIAS} and RL_{BIAS} terminals is 1.024V, then the step accuracy is 4mV.

The voltage at the RW_{BIAS} pin is then fed into the V_{BIAS} voltage follower. The V_{BIAS} pin is a buffered output that is used to drive the gate of an LDMOS transistor.

The scaling voltage, V_{REF}, set by the R_{REF} potentiometer, sets the calibrated operating point of the LDMOS Amplifier.

On edge transitions of the INC/$\overline{DEC}$ signal, the X9470 will latch the current wiper position - this is known as “Bias Lock™” mode. This is shown in Figure 6. When BiasLock occurs, the comparator hysteresis will allow INC/$\overline{DEC}$ to change state only after the IA output changes by more than 20mV. This will prevent toggling of the V_{BIAS} output unless the drain bias current is constantly changing.

State 2: DC-bias Disable When RF is Present (optional)

When an RF signal is present, the X9470 is put into standby mode (open loop). The X9470 is in standby mode when the CS pin is disabled so that the R_{BIAS} potentiometer holds the last wiper position. The presence of an RF signal at the input of a Class A or AB amplifier increases the current across the R_{sense} resistor. Over a period of time, the temperature of the LDMOS also increases and the LDMOS also experiences V_{GS} drift. Therefore the DC biasing point that was set during State 1 (calibration) is not optimal. Adjustments to the gate voltage will need to be made to optimize the operation of the LDMOS PA. This is done in State 3.

State 3: PA Standby Mode, DC Bias Adjustment [Compensation for V_{GS} Drift and Temperature Variation]

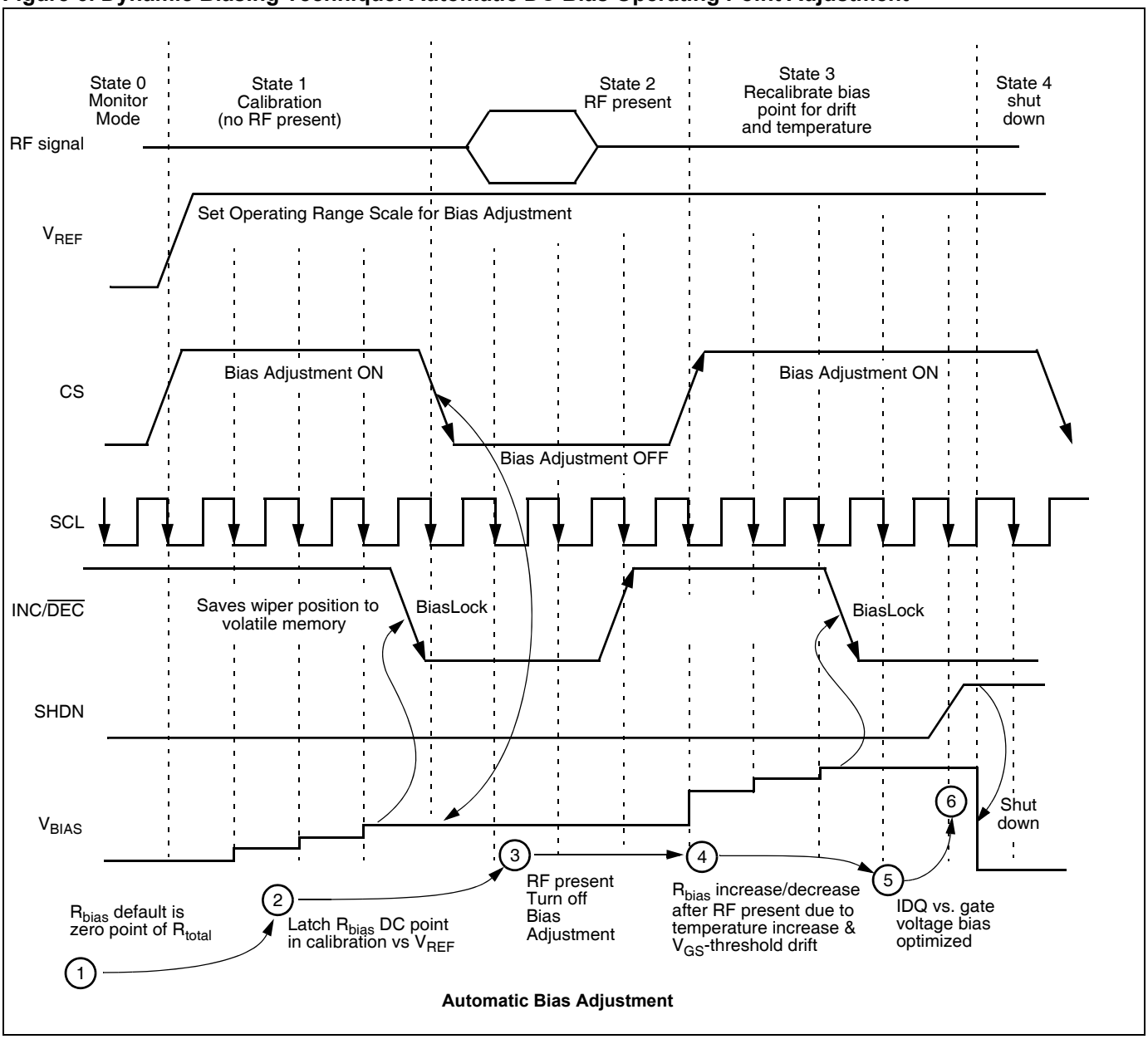
When the Power Amplifier is in Standby Mode the X9470 allows for dynamic adjustment of the DC biasing point to take into account both V_{GS} drift and temperature variation. Dynamic biasing is achieved with the X9470 by using the CS, and SCL pins. For example, the SCL pin can be a steady clock and the CS pin can be used as a control signal to enable/disable the Bias Adjustment Block.

Figure 6 illustrates how the X9470 can be used for dynamic biasing. Upon the presence of an RF signal, the CS pin is pulled LOW. This will prevent the X9470 from changing the V_{BIAS} voltage during I_{DQ} peak currents. Once the RF signal is no longer present, the CS pin can be enabled (closed loop), SDA high and the X9470 Bias Adjustment Circuit moves the V_{BIAS} voltage (the gate voltage of the FET) to meet the average I_{DQ} bias point for optimum amplifier performance.

State 4: Power Off Mode

During power saving or power-off modes the X9470 can be shut down via the SHDN pin. This pin pulls the output of the V_{BIAS} pin LOW.

Figure 6. Dynamic Biasing Technique: Automatic DC Bias Operating Point Adjustment



X9470 STATUS REGISTER (SR) AND CONTROL REGISTER (CR) INFORMATION

Table 2. Status Register (SR)

Byte Addr	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
0F hex	SHDN	INC/$\overline{DEC}$	0	CS	0	0	WEL	Gain

STATUS REGISTER (SR)

The Status Register is located at address 0F<hex>. This is a register used to control the write enable latches, and monitor status of the SHDN, INC/$\overline{DEC}$, and CS pin. This register is separate from the Control Register.

SR7: SHDN: Vbias SHDN Flag. Read Only—Volatile. The bit keeps status of the shutdown pin, SHDN. When this bit is HIGH, the SHDN pin is active and the V_{BIAS} output is disabled. When this bit is LOW, the SHDN pin is low and V_{BIAS} output is enabled.

SR6: INC/$\overline{DEC}$: Read Only—Volatile. This bit keeps status of the INC/$\overline{DEC}$ pin. When this bit is HIGH the counter is in increment mode, when this bit is LOW the counter is in decrement mode.

SR4: CS: Read Only—Volatile. This bit keeps status on the CS pin. When this bit is HIGH, the X9470 is in closed loop mode (Rbias adjustment enabled). When this bit is LOW the x9470 is in open loop mode (no Rbias adjustments).

SR2, SR3, SR5: Read only

For internal test usage, should be set to 0 during SR writes.

SR1: WEL: Write Enable Latch—Volatile

The WEL bit controls the access to the registers during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is set LOW, Nonvolatile writes to the registers will be ignored, and all writes to registers will be volatile. The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the Status Register. Once this write operation is completed and a STOP command is issued, nonvolatile writes will then occur for all NOVRAM registers and control bits. Once set, the, WEL bit remains set until either reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the Status Register) or until the part powers up again.

SR0: Gain - NOVRAM

Selects VOUT and IA gain. When SR0=0, VOUT gain = 20x, IA gain = 50x. When SR0 = 1, VOUT gain = 50x, and IA gain = 20x. Default setting is 0.

CONTROL REGISTERS (CR)

The control registers are organized for byte operations. Each byte has a unique byte address as shown in Table 3 below.

Table 3. Control Registers (CR)

Byte Addr. <HEX>	Description	Reg Name	Bit								Memory Type
			7	6	5	4	3	2	1	0	
00 hex	DCP for Vbias	Vbias	Vb7	Vb6	Vb5	Vb4	Vb3	Vb2	Vb1	Vb0	NOVRAM
01 hex	DCP for VREF	Vref	X	X	Vr5	Vr4	Vr3	Vr2	Vr1	Vr0	NOVRAM

Note: 02H to 0EH are reserved for internal manufacturing use.

X9470 BUS INTERFACE INFORMATION

Figure 7. Slave Address, Word Address, and Data Bytes - Write Mode

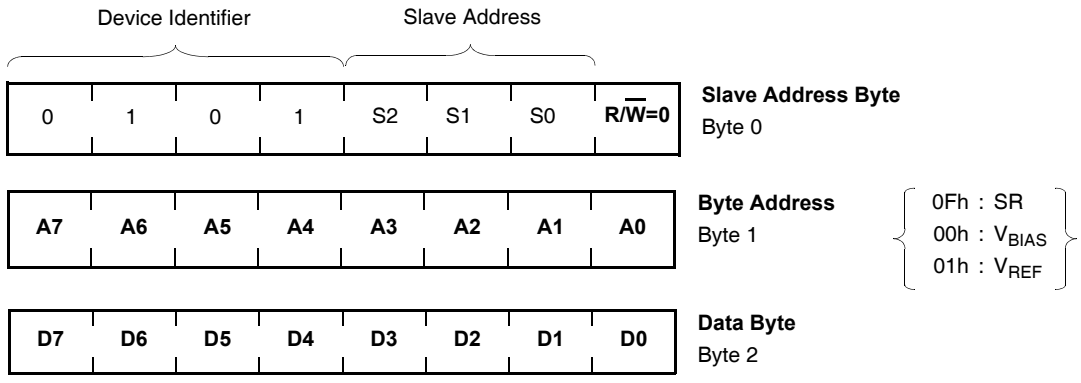
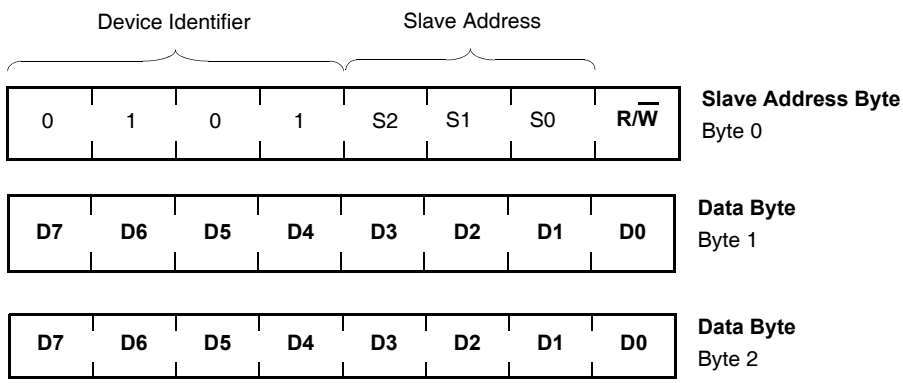


Figure 8. Slave Address, Word Address, and Data Bytes - Read Mode



Slave Address, Byte Address, and Data Byte

The byte communication format for the serial bus is shown in Figures 7 and 8 above. The first byte, BYTE 0, defines the device indentifier, 0101 in the upper half; and the device slave address in the low half of the byte. The slave address is determined by the logic values of the A0, A1, and A2 pins of the X9470. This allows for up to 8 unique addresses for the X9470. The next byte, BYTE 1, is the Byte Address. The Byte Address identifies a unique address for the Status or Control Registers as shown in Table 3. The following byte, Byte 2, is the data byte that is used for READ and WRITE operations.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 9.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 9.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 10.

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for:

– The Slave Address Byte when the Device Identifier and/or Select bits are incorrect

– The 2nd Data Byte of a Status Register Write Operation (only 1 data byte is allowed)

Figure 9. Valid Start and Stop Conditions

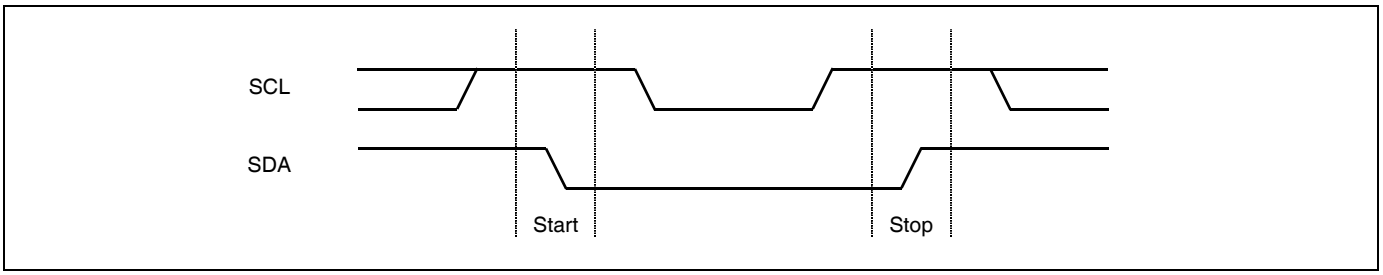


Figure 10. Acknowledge Response From Receiver

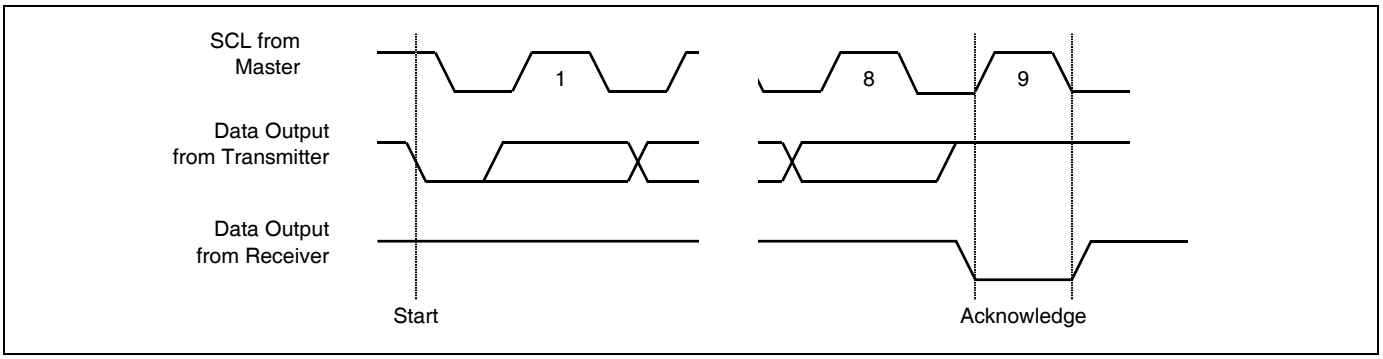
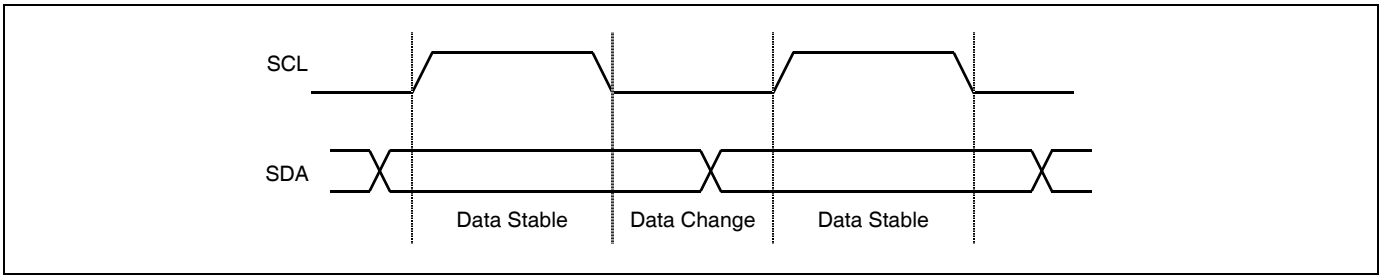


Figure 11. Valid Data Changes on the SDA Bus



WRITE OPERATIONS

Byte Write

For a write operation, the device requires the Slave Address Byte and the Word Address Bytes. This gives the master access to any one of the words in the array. Upon receipt of each address byte, the X9470 responds with an acknowledge. After receiving the address bytes the X9470 awaits the eight bits of data. After receiving the 8 data bits, the X9470 again responds with an acknowledge. The master then terminates the transfer by generating a stop condition. The X9470 then begins an internal write cycle of the data to the nonvolatile memory. During the internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 12.

A write to a protected block of memory is ignored, but will still receive an acknowledge. At the end of the write command, the X9470 will not initiate an internal write cycle, and will continue to ACK commands.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and it's associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the X9470 resets itself without performing the write. The contents of the array are not affected.

Acknowledge Polling

Disabling of the inputs during nonvolatile write cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the X9470 initiates the internal nonvolatile write cycle. Acknowledge polling can begin immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the X9470 is still busy with the nonvolatile write cycle then no ACK will be returned. When the X9470 has completed the write operation, an ACK is returned and the host can proceed with the read or write operation. Refer to the flow chart in Figure 15.

READ OPERATIONS

There are three basic read operations: Current Address Read, Random Read, and Sequential Read.

Current Address Read

Internally the X9470 contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the address is initialized to 0h. In this way, a current address read immediately after the power-on reset can download the entire contents of memory starting at the first location. Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the X9470 issues an acknowledge, then transmits eight data bits. The master terminates the read operation by not responding with an acknowledge during the ninth clock and issuing a stop condition. Refer to Figure 13 for the address, acknowledge, and data transfer sequence.

Figure 12. Byte Write Sequence

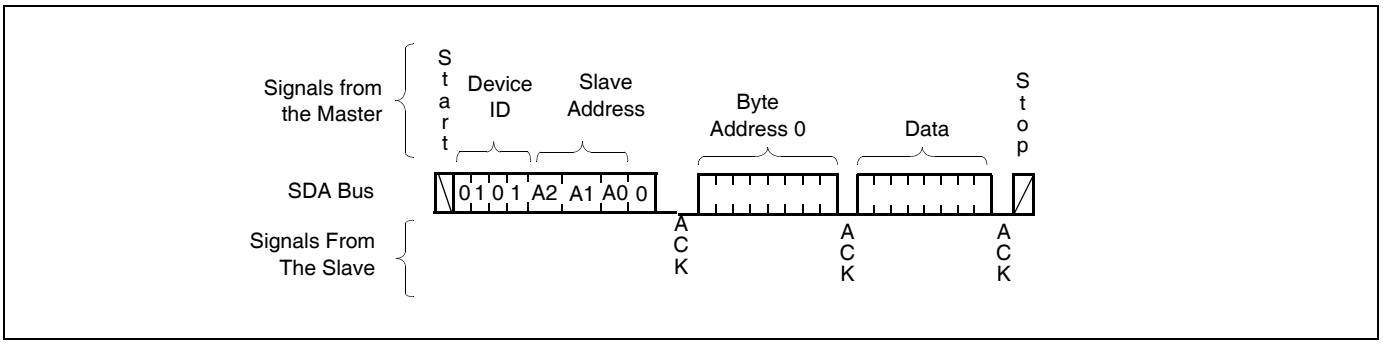


Figure 13. Current Address Read Sequence

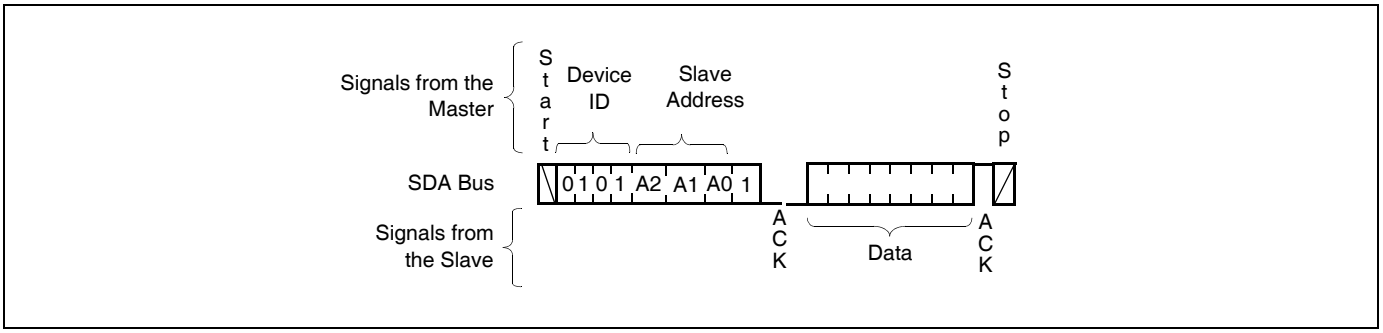


Figure 14. Random Address Read Sequence

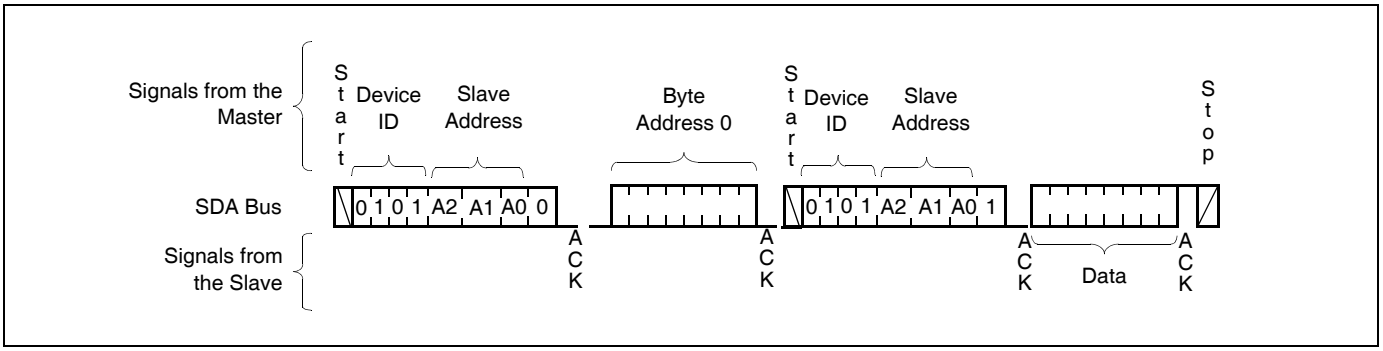
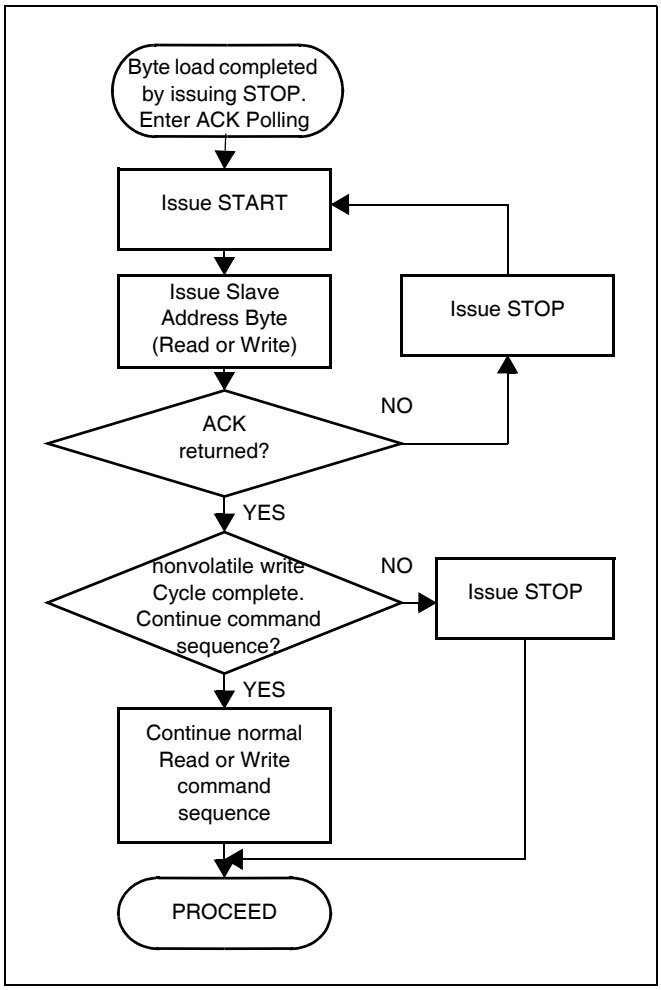


Figure 15. Acknowledge Polling Sequence



It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Random Read

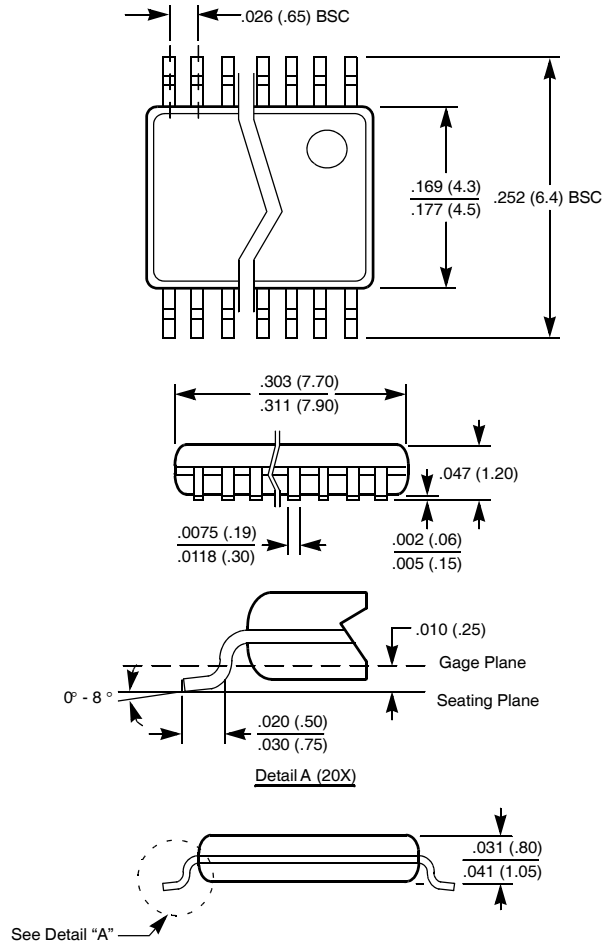
Random read operations allows the master to access any location in the X9470. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to zero, the master must first perform a “dummy” write operation.

The master issues the start condition and the slave address byte, receives an acknowledge, then issues the word address bytes. After acknowledging receipt of each word address byte, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 13 for the address, acknowledge, and data transfer sequence.

In a similar operation called “Set Current Address,” the device sets the address if a stop is issued instead of the second start shown in Figure 14. The X9470 then goes into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Current Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

PACKAGING INFORMATION

24-Lead Plastic, TSSOP Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)