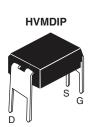
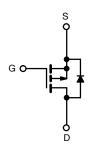
COMPLIANT

Vishay Siliconix

Power MOSFET





P-Channel MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	-10	-100				
R _{DS(on)} (Ω)	V _{GS} = -10 V	0.60				
Q _g max. (nC)	18	18				
Q _{gs} (nC)	3.0	3.0				
Q _{gd} (nC)	9.0	9.0				
Configuration	Sing	Single				

FEATURES

- · Dynamic dv/dt rating
- Repetitive avalanche rated
- For automatic Insertion
- End stackable
- P-channel
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD9120PbF

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	-100		
Gate-source voltage			V_{GS}	± 20	V	
Continuous drain current	V _{GS} at -10 V	T _A = 25 °C	- I _D	-1.0	А	
Continuous drain current		T _A = 100 °C		-0.70		
Pulsed drain current ^a			I _{DM}	-8.0		
Linear derating factor				0.0083	W/°C	
Single pulse avalanche energy ^b			E _{AS}	140	mJ	
Repetitive avalanche current a			I _{AR}	-1.0	Α	
Repetitive avalanche energy ^a			E _{AR}	0.13	mJ	
aximum power dissipation T _A = 25 °C		P_{D}	1.3	W		
Peak diode recovery dv/dt ^c			dv/dt	-5.5	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +175	°C	
Soldering rRecommendations (peak temperature) ^d	For 10 s			300		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = -25 V, starting T_J = 25 °C, L = 52 mH, R_g = 25 Ω , I_{AS} = -2.0 A (see fig. 12)
- c. $I_{SD} \le -6.8 \text{ A}$, di/dt $\le 110 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 175 \text{ °C}$
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum junction-to-ambient	R _{thJA}	-	120	°C/W		

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-100	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = -1 mA	-	-0.10	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = -250 μA	-2.0	-	-4.0	V
Gate-source leakage	I _{GSS}		V _{GS} = ± 20 V	-	-	± 100	nA
	I _{DSS}	V _{DS} = -100 V, V _{GS} = 0 V		-	-	-100	μА
Zero gate voltage drain current		$V_{DS} = -80 \text{ V}$	V _{DS} = -80 V, V _{GS} = 0 V, T _J = 150 °C		-	-500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -0.6 A ^b	-	-	0.60	Ω
Forward transconductance	9 _{fs}	$V_{DS} = -$	50 V, I _D = -0.60 A b	0.71	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V		-	390	-	pF
Output capacitance	C _{oss}		$V_{DS} = -25 \text{ V}$ f = 1.0 MHz, see fig. 5		170	-	
Reverse transfer capacitance	C _{rss}	f = 1			45	-	
Total gate charge	Qg			-	-	18	nC
Gate-source charge	Q_{gs}	$V_{GS} = -10 \text{ V}$	$V_{GS} = -10 \text{ V}$ $I_D = -6.8 \text{ A}, V_{DS} = -80 \text{ V}$ see fig. 6 and 13 b		-	3.0	
Turn-on delay time	Q_{gd}	see lig. 6 and 13		=	-	9.0	
Rise time	t _{d(on)}	V_{DD} = -50 V, I_{D} = -6.8 A R_{g} = 18 Ω , R_{D} = 7.1 Ω , see fig. 10 ^b		-	9.6	-	ns
Turn-off delay time	t _r			=	29	-	
Fall time	t _{d(off)}			=	21	-	
Turn-on delay time	t _f			-	25	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	- LI
Internal source inductance	L _S			-	6.0	-	- nH
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-1.0	А
Pulsed diode forward current ^a	I _{SM}			-	-	-8.0	
Body diode voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = -1.0 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	-6.3	V
Body diode reverse recovery time	t _{rr}	T 05.00 !	0.0 A 31/31 400 A / b	-	98	200	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = -6.8 \text{A}, \text{di/dt} = 100 \text{A/} \mu \text{s}^{ \text{b}}$		-	0.33	0.66	μC
Forward turn-on time	t _{on}	Intrinsic tu	rn-on time is negligible (turn	on is dor	ninated b	y L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

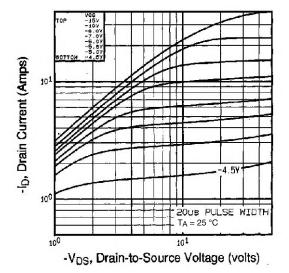


Fig. 1 - Typical Output Characteristics, $T_A = 25$ °C

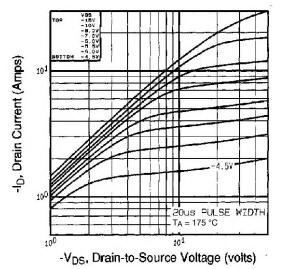


Fig. 2 - Typical Output Characteristics, T_A = 175 °C

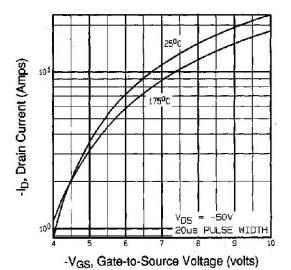


Fig. 3 - Typical Transfer Characteristics

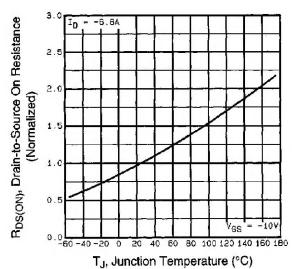


Fig. 4 - Normalized On-Resistance vs. Temperature



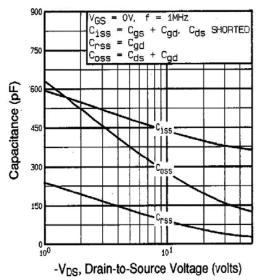


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

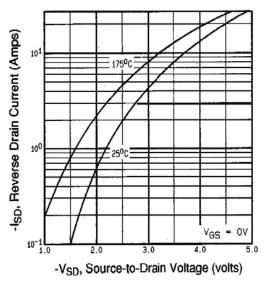


Fig. 7 - Typical Source-Drain Diode Forward Voltage

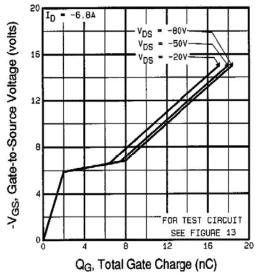


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

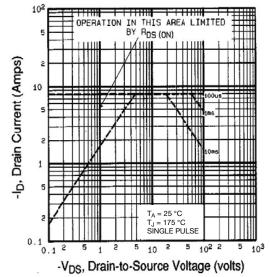


Fig. 8 - Maximum Safe Operating Area



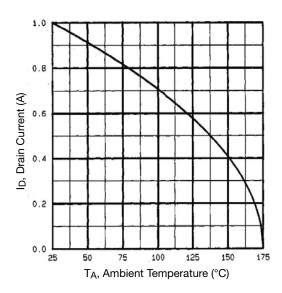


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

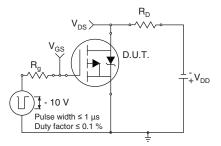


Fig. 10a - Switching Time Test Circuit

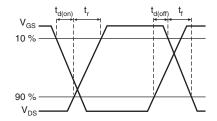


Fig. 10b - Switching Time Waveforms

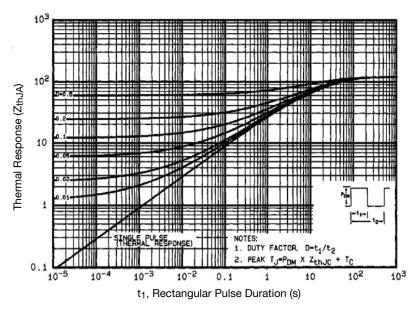


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



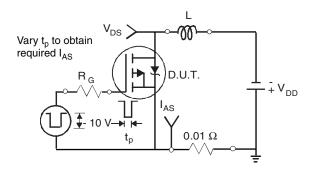


Fig. 12a - Unclamped Inductive Test Circuit

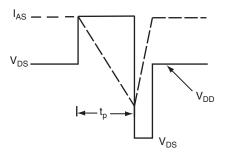


Fig. 12b - Unclamped Inductive Waveforms

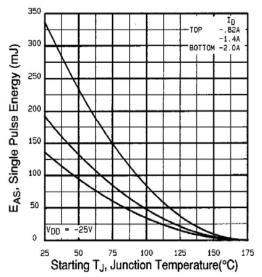


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

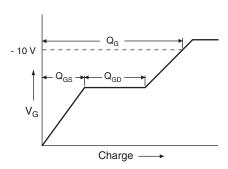


Fig. 13a - Basic Gate Charge Waveform

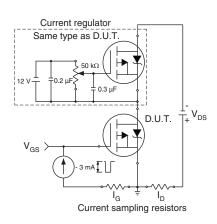
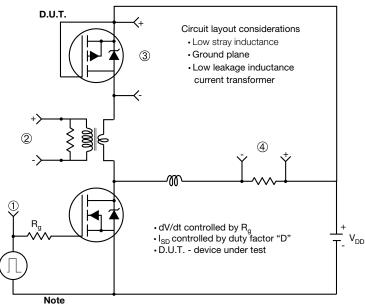


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver

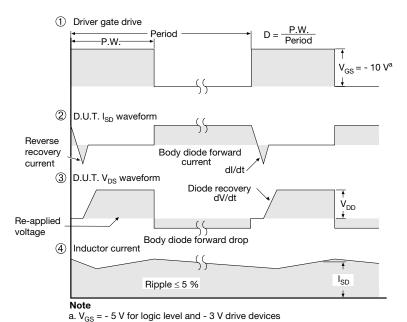
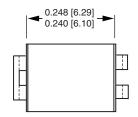


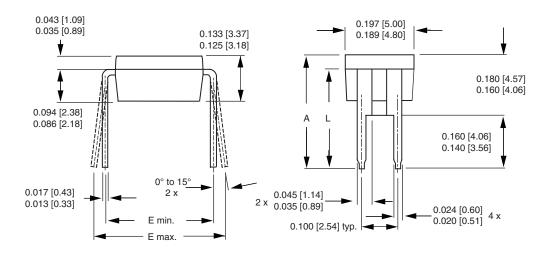
Fig. 14 - For P-Channel

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Vishay Siliconix

HVM DIP (High voltage)





	INCHES		MILLIMETERS		
DIM.	MIN.	MAX.	MIN.	MAX.	
A	0.310	0.330	7.87	8.38	
Е	0.300	0.425	7.62	10.79	
L	0.270	0.290	6.86	7.36	

ECN: X10-0386-Rev. B, 06-Sep-10

DWG: 5974

Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

Document Number: 91361 Revision: 06-Sep-10



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