Click here for production status of specific part numbers.

MAX86916 Integrated Optical Sensor Module for Mobile Health

General Description

The MAX86916 is an integrated optical sensor platform with applications in bio-sensing, proximity, and color. It includes internal LEDs, photodetectors, and low-noise electronics with ambient-light-rejection circuitry. The MAX86916 helps ease design-in effort to all mobile and wearable devices.

The MAX86916 operates on a 1.8V supply voltage, with a separate 5.5V power supply for the internal LEDs. Communication to and from the module is accomplished entirely through a standard I²C-compatible interface. The module can be shut down through software with near-zero standby current, allowing the power rails to remain powered at all times.

Applications

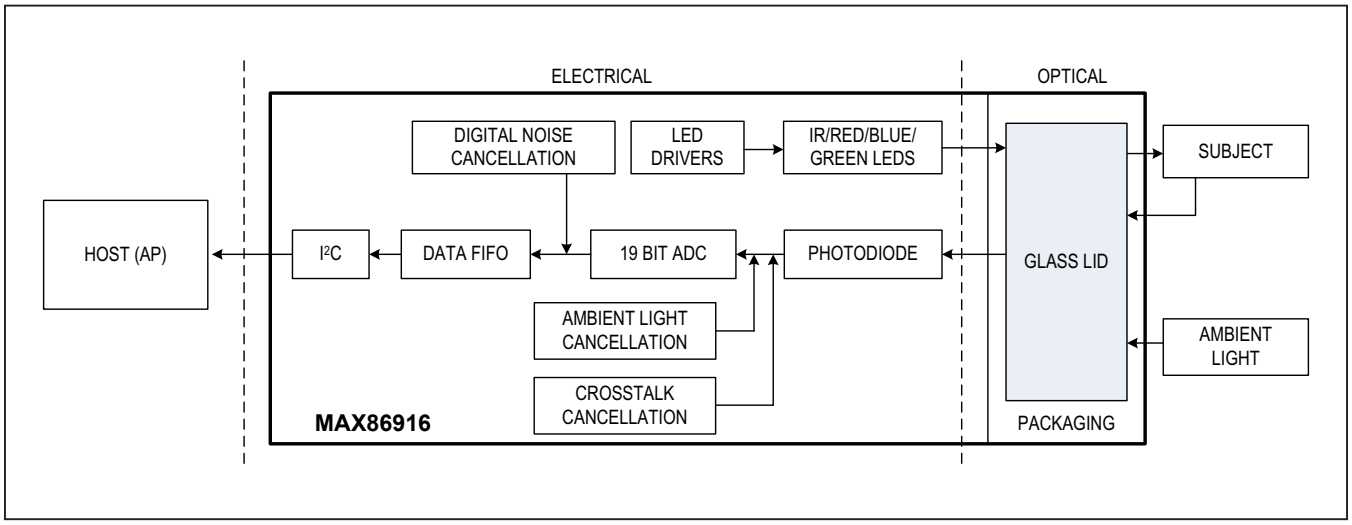
- Smartphones/Accessories
- Tablets
- Wearable Devices
- Fitness Assistant Devices

Benefits and Features

- Miniature 3.5mm x 7.0mm x 1.5mm, 14-Pin Optical Module
- Optical-Grade Glass for Long-Term Optimal and Robust Performance
- Ultra-Low-Power Operation for Mobile Device
- Ultra-Low Shutdown Current (0.7µA, Typical)
- Built-In Low Noise Crosstalk Cancellation
- -40°C to +85°C Operating Temperature Range
- Reflective Heart Rate Monitor, Medical-Grade Pulse Oximeter, and Bio-Optical Sensor Platform

Ordering Information *appears at end of data sheet.*

Simplified Block Diagram



Absolute Maximum Ratings

VDD to GND .....-0.3V to +2.2V
PGND to GND .....-0.3V to +0.3V
VLED to PGND.....-0.3V to +6.0V
LED_DRV1 to PGND .....-0.3V to V_{LED}+0.3V
LED_DRV2 to PGND .....-0.3V to V_{LED}+0.3V
LED_DRV3 to PGND .....-0.3V to V_{LED}+0.3V
LED_DRV4 to PGND .....-0.3V to V_{LED}+0.3V
VREF to GND.....-0.3V to +2.2V
All other pins to GND .....-0.3V to +6V

Output Short-Circuit Duration .....Continuous
Continuous Input Current Into Any Pin (except LED_DRVx Pins) .....±20mA
Continuous Power Dissipation (derate 3.25mW/°C above +70°C) 300mW
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -40°C to +105°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 14 OLGA	
Package Code	F143B7MK+1
Outline Number	**21-100325**
Land Pattern Number	**90-100122**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	125.6°C/W
Junction to Case (θ_{JC})	123.1°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 1.8V, V_{LED} = 5V, LED_PW = 70µs, SR = 1000sps, ADC_RGE = 32µA, LEDx_RGE = 50mA, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, Note 1).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power Supply Voltage	V_{DD}	Verified during PSRR Test		1.7	1.8	2.0	V
LED Supply Voltage (Note 2)	V_{LED}	Verified during PSRR Test		3.5		5.5	V
Supply Current	I_{DD}	LEDx_PA = 0x00, LED_PW = 220µS, SR = 100sps	One LED Exposure/Sample		410		µA
			Two LED Exposures/Sample		420		
			Three LED Exposures/Sample		440		
			Four LED Exposures/Sample		450	750	
LED Supply Current	I_{LED}	LEDx_PA = 0x00, LED_PW = 220µS, SR = 100sps	One LED Exposure/Sample		0.2		µA
			Four LED Exposures/Sample		0.6	2	
		LEDx_PA = 0xFF, LED_PW = 220µS, SR = 100sps	One LED Exposure/Sample		1300		
			Four LED Exposures/Sample		5400		

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5V, LED_PW = 70µs, SR = 1000sps, ADC_RGE = 32µA, LEDx_RGE = 50mA, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, Note 1).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current in Shutdown	I_{DDSHDN}	SHUTDOWN = 1			0.7	20	µA
LED Supply Current in Shutdown	$I_{LEDSHDN}$	SHUTDOWN = 1			0.7	1	µA
VREF	VREF			1.195	1.210	1.220	V
OPTICAL SENSOR CHARACTERISTICS							
ADC Full-Scale Range	ADC FS				4, 8, 16, 32		µA
ADC Resolution	ADC RES				19		bits
Sampling Clock Frequency	CLK			31.36	32.0	32.64	kHz
Dark Current Count	LED_DCC	LEDx_PA = 0x00, LED_PW = 420µs, SR = 100sps, ADC_RGE = 4µA			10	128	Counts
					0.002	0.025	% of FS
Ambient Light Detect Noise	Amb_ Light_Det_ Noise	LEDx_PA = 0x00, LED_PW = 420µs, AMB_LIGHT_ DET = 0x1, SR = 100 sps, ADC FS = 4µA, T_A = +25°C			170	384	Counts
Blue ADC Count	$BLUE_C$	Propriety ATE setup, LED_RGE = 150mA, SR = 1600sps, T_A = +25°C	LED4_PA = 0x5F	-15%	115k	+15%	Counts
			LED4_PA = 0xBF	-15%	190k	+15%	
			LED4_PA = 0xFF	-15%	235k	+ 15%	
Green ADC Count	$GREEN_C$	Propriety ATE setup, LED_RGE = 150mA, SR = 1600sps, T_A = +25°C	LED3_PA = 0x5F	-15%	95k	+15%	
			LED3_PA = 0xBF	-15%	160k	+15%	
			LED3_PA = 0xFF	-15%	200k	+15%	
Red ADC Count	RED_C	Propriety ATE setup, LED_RGE = 150mA, SR = 1600sps, T_A = +25°C	LED2_PA = 0x5F	-15%	135k	+15%	
			LED2_PA = 0xBF	-15%	265k	+15%	
			LED2_PA = 0xFF	-15%	350k	+15%	
IR ADC Count	IR_C	Propriety ATE setup, LED_RGE = 150mA, SR = 1600sps, T_A = +25°C	LED1_PA = 0x5F	-15%	160k	+15%	
			LED1_PA = 0xBF	-15%	310k	+15%	
			LED1_PA = 0xFF	-15%	400k	+15%	
ADC Count - PSRR (VDD)	$PSRR_{VDD}$	Propriety ATE setup,LEDx_RGE = 100mA, LEDx_PA = 0xFF	1.7V < V_{DD} < 2.0V		0.25	2	% of FS
		LEDx_RGE = 150mA, LED_PW = 120µs, ADC = 16µA	Frequency = DC to 100kHz, 100mV_{P-P}		30		LSB

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5V, LED_PW = 70µs, SR = 1000sps, ADC_RGE = 32µA, LEDx_RGE = 50mA, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, Note 1).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Count - PSRR (VLED) (Note 2)	$PSRR_{VLED}$	Propriety ATE setup, LEDx_RGE = 100mA, LEDx_PA = 0xFF	For IR/RED 3.5V < V_{LED+} < 5.5V		0.05	1	% of FS
			For Green/Blue 4.5V < V_{LED+} < 5.5V		0.05	1	
		LEDx_RGE = 150mA, LED_PW = 120µs, ADC = 16µA	Frequency = DC to 100kHz, 100mV_{P-P}		40		LSB
Max. DC Ambient Light Rejection	ALR	16 KLUX(QTH Lamp) directly on sensor, T_A = +25°C			200		uA
CROSSTALK CANCELLATION DAC							
Crosstalk Cancellation Range	XTALK RANGE			0		1/2 ADC FS	uA
Crosstalk Cancellation Resolution	XTALK RES				5		bit
Maximum Crosstalk Cancellation Counts	XTALK COUNTS	XTALK_CANCEL = 0x1F, LED_PW = 120µs, ADC_RGE = 16µA, LEDx_RGE = 150mA, LED1_PA = 0x70 LED2_PA = 0x80, LED3_PA = 0xF0, LED4_PA = 0xD0		-5%	253,952	+5%	Counts
Maximum Crosstalk Noise Contribution	XTALK NOISE	LED_PW = 120µs, SR = 400 sps, ADC_RGE = 16µA, LEDx_RGE = 150mA			0.3		dB
LED DRIVERS							
Maximum LED Drive Current and Headroom Voltage	I_{LED}, VLED_headroom	LEDx_RGE<1:0> = 00			50, 0.15		mA, V
		LEDx_RGE<1:0> = 01			100, 0.3		
		LEDx_RGE<1:0> = 10			150, 0.44		
LED Current Resolution					8		Bits
LED Pulse Width	INT	LED_PW<1:0> = 0x00			70		µs
		LED_PW<1:0> = 0x01			120		
		LED_PW<1:0> = 0x10			220		
		LED_PW<1:0> = 0x11			420		
IR LED CHARACTERISTICS (Note 3)							
Centroid Wavelength	$\lambda_{centroid}$	I_F = 100mA, tp = 10ms, T_A = +25°C		930		955	nm
Forward Voltage	V_F	I_F = 100mA, tp = 10 ms, T_A = +25°C			1.6	1.8	V
Radiant Power	Φ_e	I_F = 100mA, T_A = +25°C			60		mW
Maximum Forward Current		T_A = +25°C				100	mA
Maximum Junction Temperature	T_J					125	°C

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5V, LED_PW = 70µs, SR = 1000sps, ADC_RGE = 32µA, LEDx_RGE = 50mA, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, Note 1).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RED LED CHARACTERISTICS (Note 3)						
Centroid Wavelength	$\lambda_{centroid}$	I_F = 50mA, T_A = +25°C	655		663	nm
Forward Voltage	V_F	I_F = 50 mA, tp = 5 ms, T_A = +25°C	1.90	2.30	2.40	V
Radiant Power	Φ_e	I_F = 20 mA, T_A = +25°C		6.4		mW
Maximum Forward Current		T_A = +25°C			70	mA
Maximum Junction Temperature	T_J				125	°C
GREEN LED CHARACTERISTICS (Note 3)						
Centroid Wavelength	$\lambda_{centroid}$	I_F = 140mA, tp = 10 ms, T_A = +25°C	520		535	nm
Forward Voltage	V_F	I_F = 140 mA, tp = 5 ms,, T_A = +25°C	3.1	3.5	3.9	V
Radiant Power	Φ_e	I_F = 20mA, T_A = +25°C		6		mW
Maximum Forward Current		T_A = +25°C			140	mA
Maximum Junction Temperature	T_J				150	°C
BLUE LED CHARACTERISTICS (Note 3)						
Centroid Wavelength	$\lambda_{CENTROID}$	I_F = 20mA, tp = 10 ms, T_A = +25°C	455		466	nm
Forward Voltage	V_F	I_F = 20 mA, tp = 5 ms,, T_A = +25°C	2.70	2.85	3.30	V
Radiant Power	Φ_E	I_F = 20 mA, T_A = +25°C		10		mW
Maximum Forward Current		T_A = +25°C			60	mA
Maximum Junction Temperature	T_J				125	°C
PHOTODIODE (Note 3)						
Spectral Range of Sensitivity	$L_{10\%}$			400 … 1100		nm
Radiant Sensitive Area	A			1.51		mm^2
Photo Diode Dark Current	I_{PD_DARK}	Vr = 5V			5	nA
DIGITAL CHARACTERISTICS (SDA, SCL, INTB)						
Output Low Voltage SDA, INTB	V_{OL}	I_{SINK} = 6mA			0.4	V
I2C Input Voltage Low	V_{IL_I2C}	SDA, SCL			0.4	V
I2C Input Voltage High	V_{IH_I2C}	SDA, SCL	1.4			V
Input Hysteresis	V_{HYS}	SDA, SCL		200		mV
Input Capacitance	C_{IN}	SDA, SCL		10		pF
Input Leakage Current	I_{IN}	V_{IN} = 0V, T_A = +25°C (SDA, SCL, INTB)		0.01	1	µA
		V_{IN} = 5.5V, T_A = +25°C (SDA, SCL, INTB)		0.01	1	

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5V, LED_PW = 70µs, SR = 1000sps, ADC_RGE = 32µA, LEDx_RGE = 50mA, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, Note 1).

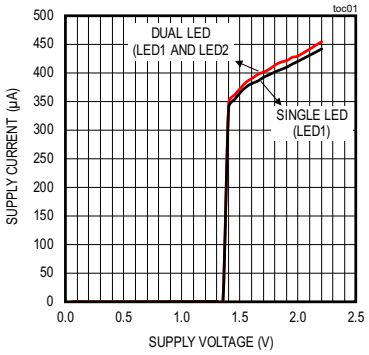
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING CHARACTERISTICS (SDA, SCL) (Note 4)						
I²C Write Address				AE		Hex
I²C Read Address				AF		Hex
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Bus Capacitance	C_B				400	pF
SDA and SCL Receiving Rise Time	t_R			20 + 0.1CB	300	ns
SDA and SCL Receiving Fall Time	t_F			20 + 0.1CB	300	ns
SDA Transmitting Fall Time	t_F			20 + 0.1CB	300	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.
Note 2: V_{LED} should be set to accommodate the maximum LED forward voltage and the output compliance of the LED driver.
Note 3: For design guidance only. Not production tested. Tested in die only.
Note 4: For design guidance only. Not production tested.

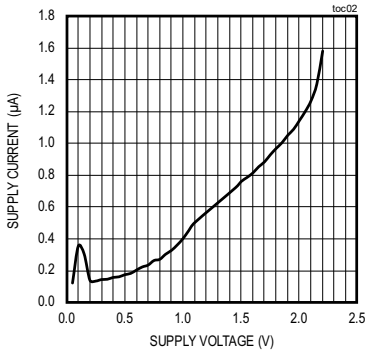
Typical Operating Characteristics

V_{DD} = +1.8V, V_{LED} = +5V, T_A = +25°C, unless otherwise noted.

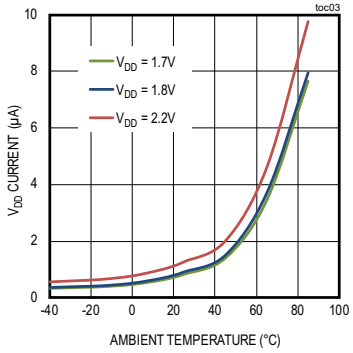
V_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE SAMPLE RATE = 100Hz



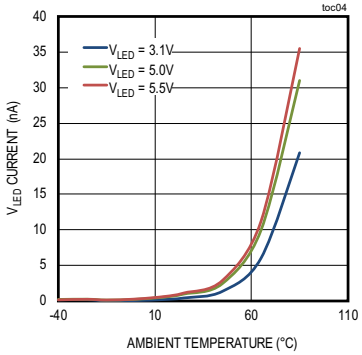
V_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE SHUTDOWN MODE



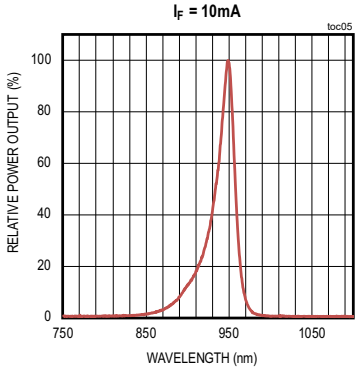
AVERAGE V_{DD} SHUTDOWN CURRENT vs. TEMPERATURE



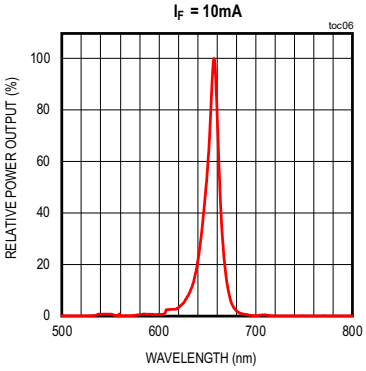
AVERAGE V_{LED} SHUTDOWN CURRENT vs. TEMPERATURE



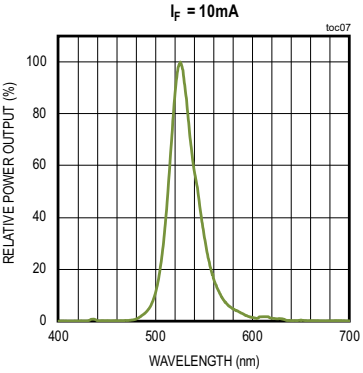
NORMALIZED IR LED SPECTRUM I_F = 10mA



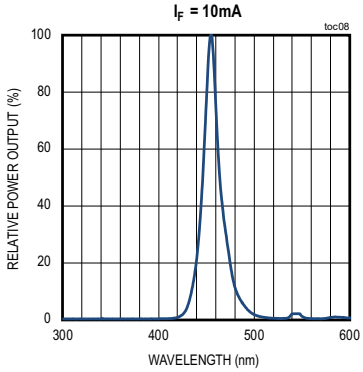
NORMALIZED RED LED SPECTRUM I_F = 10mA



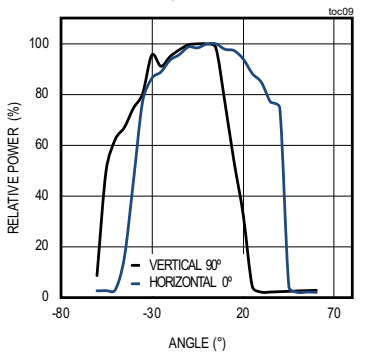
NORMALIZED GREEN LED SPECTRUM I_F = 10mA



NORMALIZED BLUE LED SPECTRUM I_F = 10mA



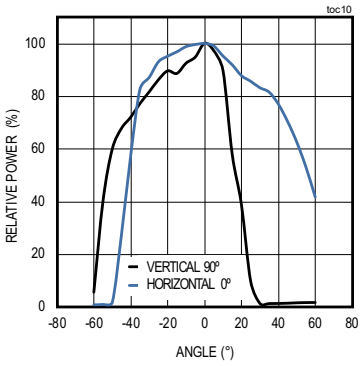
IR LED RADIATION PATTERN NORMALIZED



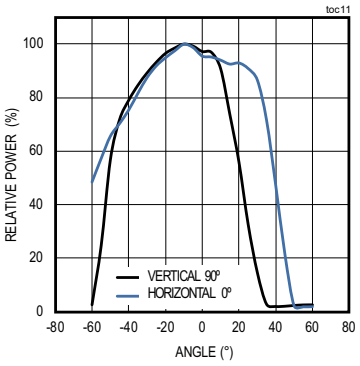
Typical Operating Characteristics (continued)

V_{DD} = +1.8V, V_{LED} = +5V, T_A = +25°C, unless otherwise noted.

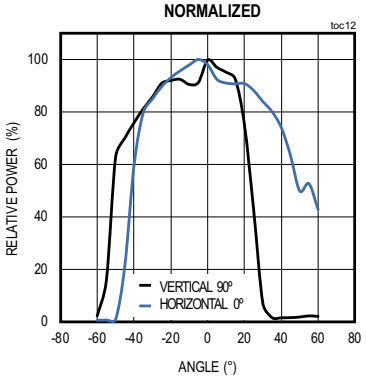
RED LED RADIATION PATTERN
NORMALIZED



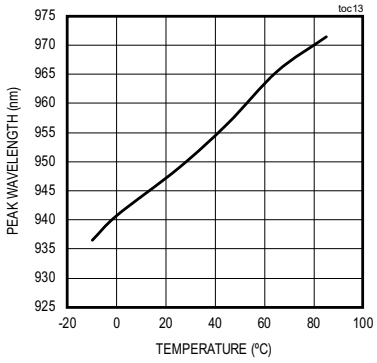
GREEN LED RADIATION PATTERN
NORMALIZED



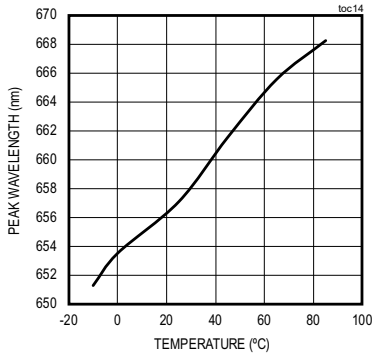
BLUE LED RADIATION PATTERN
NORMALIZED



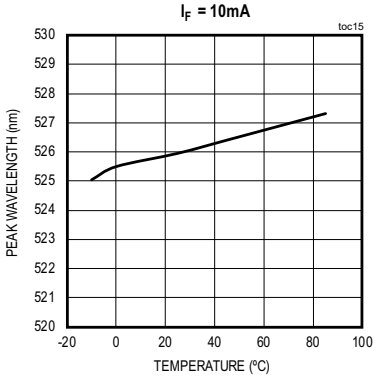
IR LED PEAK WAVELENGTH
vs. TEMPERATURE



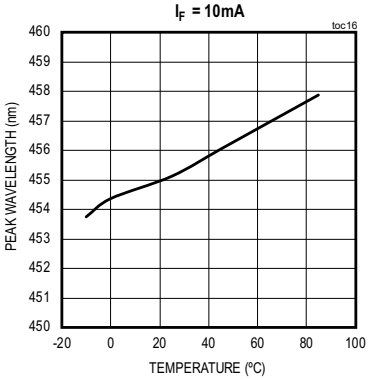
RED LED PEAK WAVELENGTH
vs. TEMPERATURE



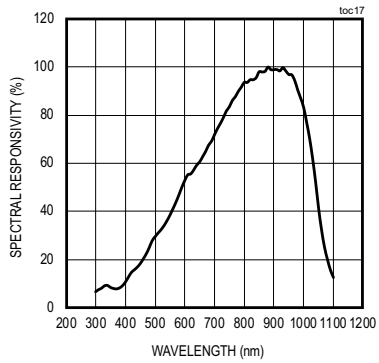
GREEN LED PEAK WAVELENGTH
vs. TEMPERATURE
I_F = 10mA



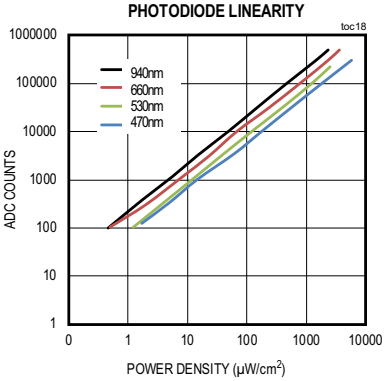
BLUE LED PEAK WAVELENGTH
vs. TEMPERATURE
I_F = 10mA



NORMALIZED
SPECTRAL RESPONSIVITY



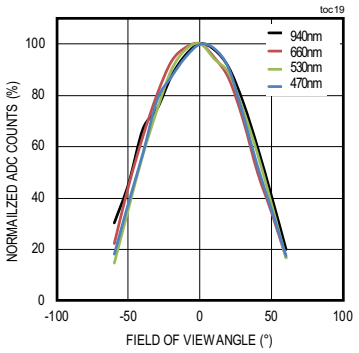
PHOTODIODE LINEARITY



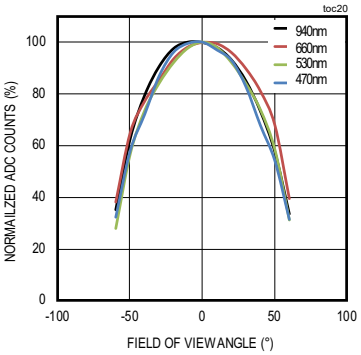
Typical Operating Characteristics (continued)

V_{DD} = +1.8V, V_{LED} = +5V, T_A = +25°C, unless otherwise noted.

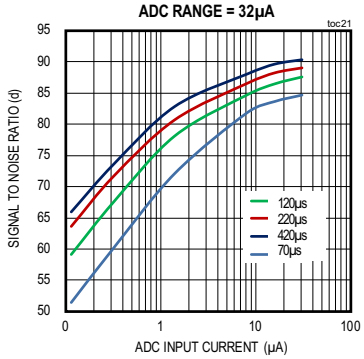
PHOTODIODE FIELD OF VIEW
NORMALIZED HORIZONTAL 0° ORIENTATION



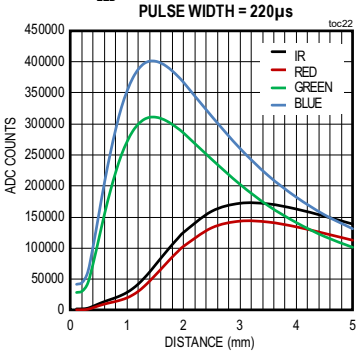
PHOTODIODE FIELD OF VIEW NORMALIZED
VERTICAL 90° ORIENTATION



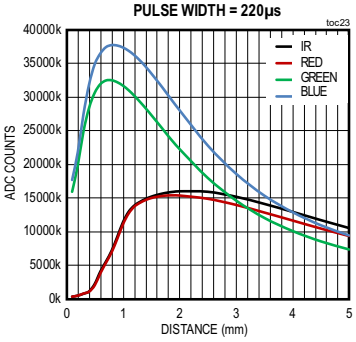
SIGNAL TO NOISE RATIO
vs. ADC INPUT CURRENT
ADC RANGE = 32µA



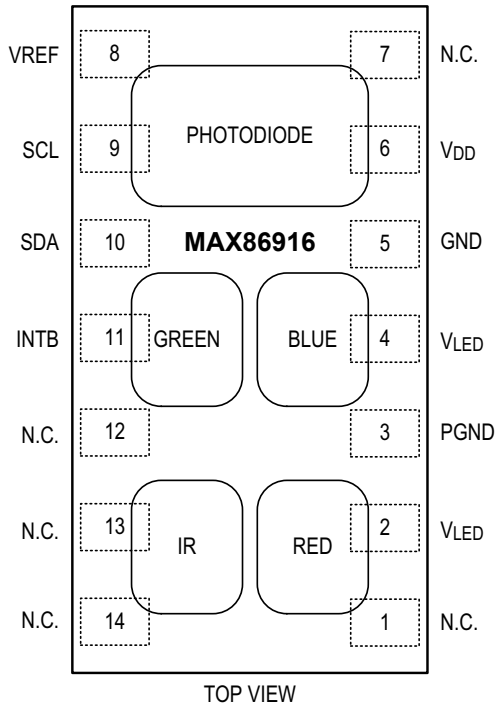
DC COUNTS vs. DISTANCE
WHITE CARD REFLECTOR
I_{LED} = 10mA, SAMPLE RATE = 100Hz,
PULSE WIDTH = 220µs



DC COUNTS vs. DISTANCE
COVER GLASS
I_{LED} = 10mA, SAMPLE RATE = 100Hz,
PULSE WIDTH = 220µs



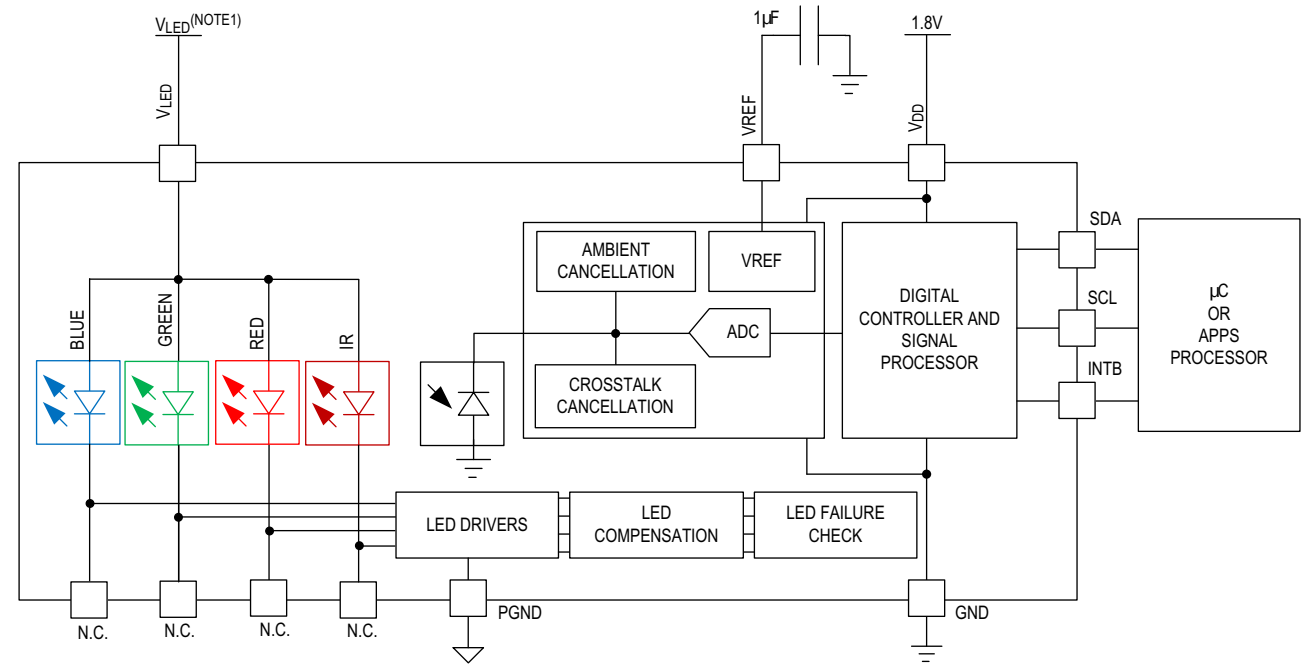
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
POWER		
6	V_{DD}	Main Power Supply. Connect to externally-regulated supply. Bypass with a 0.1µF capacitor as close as possible to pad and a 4.7µF capacitor to GND.
5	GND	Main Power Return. Connect to GND.
4, 2	V_{LED}	LED Power Supply Input. Connect to external voltage supply. Bypass with a 0.1µF capacitor as close as possible to pad and a 10µF capacitor to GND.
3	PGND	LED Power Return. Connect to GND.
CONTROL INTERFACE		
10	SDA	SDA Input/Output. I^2C data I/O
9	SCL	SCL Input. I^2C clock input
11	INTB	Interrupt. Programmable open-drain interrupt output signal (active-low).
REFERENCE		
8	VREF	Internal Reference Decoupling Point. Bypass with a 1µF capacitor to GND.
N.C.		
1, 12, 13, 14	N.C.	No Connection. Internally connected to LEDx cathode (x = 1–4). Leave N.C. unconnected.
7	N.C.	No Connection. Internally connected. Leave N.C. unconnected.

Functional Diagrams



NOTE 1: IF GREEN/BLUE LED IS USED, V_{LED} MUST BE 5.0V OR ABOVE.

Detailed Description

The MAX86916 is an optical sensor module designed for the demanding requirements of mobile devices. The MAX86916 maintains a very small total solution size without sacrificing optical or electrical performance. Minimal external hardware components are necessary for integration into a mobile device.The MAX86916 is fully adjustable through software registers, and the digital output data is stored in a 32-deep FIFO within the device. The FIFO allows the MAX86916 to be connected to a microcontroller or processor on a shared bus, where the data is not being read continuously from the MAX86916 registers.

Photo Diode Receiver

The receive path in the MAX86916 is composed of an ambient-light-cancellation (ALC) circuit, a continuous-time sigma-delta ADC, and proprietary digital filter that rejects slow-changing ambient light, including 100Hz/120Hz interference from artificial lights. The ALC uses a track-and-hold to cancel ambient light.The internal ADC is a continuous time oversampling sigma delta converter with 19-bit resolution. The ADC output data rate can be programmed from 50sps (samples per second) to 3200sps.

The optical subsystem in MAX86916 is features a proprietary ambient-light-cancellation (ALC) circuit. This ALC scheme is designed to cancel ambient-light-generated photo diode current up to 200µA, allowing the sensor to work in high ambient light conditions.

When the ambient light cancellation function has reached its maximum limit due to overflow from strong ambient light, the output of the ADC could be affected. In this case, Ambient Light Cancellation Overflow interrupt (ALC_OVF) can be used to detect the condition. This interrupt can be enabled by setting Ambient Light Cancellation Overflow Interrupt enable (ALC_OVF_EN).

By default, ALC is enabled. But if a measurement of direct ambient light is needed, ALC can be disabled. This can be done by enabling “Ambient Light Detection Mode” (AMB_LIGHT_DET = 1). In this mode, the filtering scheme used for ALC will be disabled. To measure ambient light correctly, LED Current Pulse Amplitude (LEDx_PA) should also be set to 0x0.

LED Driver

The MAX86916 integrates four LED drivers and BLUE, GREEN, RED, and INFRARED LEDs. The LED current can be programmed from 0mA to 150mA with proper VLED supply voltage. The LED pulse width can be programmed from 70µs to 420µs to allow the algorithm to optimize data acquisition accuracy and power consumption based on use cases.

Proximity Function

The MAX86916 includes a proximity function to save power and reduce visible light emission when the user's finger is not on the sensor. The proximity function is enabled by setting PROX_INT_EN to 1. When the programmed data acquisition is initiated, the LED1 is turned on in proximity mode with a driver current set by the PILOT_PA register. When an object is detected and ADC count exceeds the Proximity Mode Threshold. PROX_INT interrupt is asserted, FIFO_DATA is flushed and the part transitions automatically to the programmed data acquisition mode based on settings in MODE register. When the ADC count is detected below the Proximity Mode Threshold, the proximity function will be re-entered automatically without triggering the PROX_INT interrupt. The Proximity Mode threshold is defined by register PROX_INT_THRESH multiplied by 2048.

The proximity function can be disabled by resetting PROX_INT_EN to 0. In that case, when the programmed data acquisition mode is initiated in the FIFO Data Control registers, the data acquisition begins immediately.

Cross Talk Cancellation

MAX86916 features a Cross-Talk Cancellation DAC to improve the robustness of optical system design. The DAC code is used to subtract a DC component of the received optical signal at the photodetector that is coherent with the LED pulse. The intent of this feature is to cancel out the cross-talk caused by the system level optical design, especially when high reflective or translucent cover glass is used. The final optical system design will need to be characterized to set the code for XTALK_DACx.

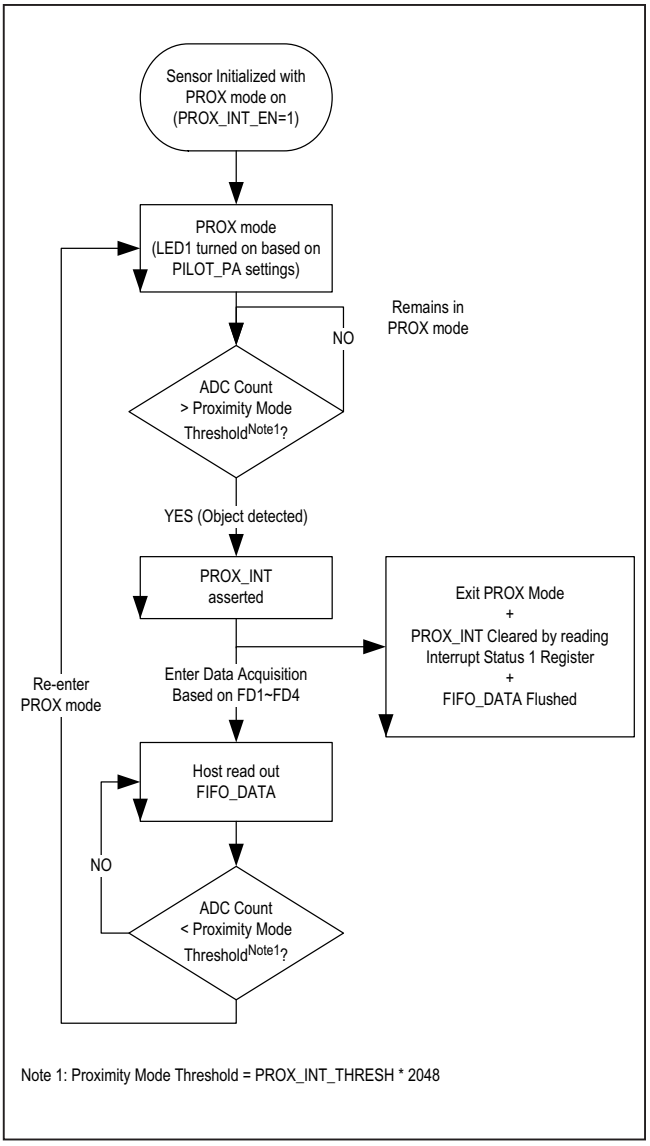


Figure 1. Proximity Function Flow Diagram

FIFO Configuration

The FIFO can hold up to 32 samples of data, each sample can be comprised of up to 4 data items (time slots). Each data item is 3 bytes. The content of each data item is programmed through registers LEDC1 to LEDC4 (LED sequence registers). These data items are ADC counts from the analog front-end of this device. The FIFO supports the following features:

- Maximum 32 samples (depth)
- Supports up to four data items in each sample
- FIFO roll-on-full
- Different interrupt modes based on watermark

There are seven registers that control how the FIFO is configured and read out. These registers are illustrated on Table 1.

LED Sequence Register, LEDCx

LED sequence registers are only effective when the MODE[1:0] is set to 0x03 (Flex LED mode). The data format in the FIFO, as well as the sequencing of exposures, are controlled by the LED sequence registers through LEDC1–LEDC4. There are four data items available, each holding up to 32 samples. The exposure sequence cycles through the LED sequence registers, starting from LEDC1 to LEDC4. The first LED sequence field set to NONE (0000) ends the sequence. Table 2 shows all the available data item types.

The LED sequence registers LEDC1, LEDC2, LEDC3, and LEDC4 control the turn-on and sequencing of the LED drivers. For settings 0x1 to 0x4, the PA setting for the enabled LED driver is read as normal from the corresponding LEDx_ PA register but for settings 0x5 to 0x8 the PA is used from the PILOT_PA register.

Table 1. FIFO Information, Control and Configuration Registers

ADDRESS	REGISTER NAME	DEFAULT VALUE	B7	B6	B5	B4	B3	B2	B1	B0
0x04	FIFO Write Pointer	00	-	-	-	FIFO_WR_PTR[4:0]				
0x05	Overflow Counter	00	-	-	-	OVF_COUNTER[4:0]				
0x06	FIFO Read Pointer	00	-	-	-	FIFO_RD_PTR[4:0]				
0x07	FIFO Data Register	00	FIFO_DATA[7:0]							
0x08	FIFO Configuration	0F	SMP_AVE[2:0]			FIFO_RO	FIFO_A_FULL[3:0]			
0x13	LED Sequence Register 1	00	LEDC2[3:0]				LEDC1[3:0]			
0x14	LED Sequence Register 2	00	LEDC4[3:0]				LEDC3[3:0]			

Table 2. LED Sequence Data Item Types

LEDCX[3:0], X = 1, 2, 3, 4	DATA ITEM TYPE
0000	OFF
0001	LED1
0010	LED2
0011	LED3
0100	LED4

LEDCX[3:0], X = 1, 2, 3, 4	DATA ITEM TYPE
0101	PILOT LED1
0110	PILOT LED2
0111	PILOT LED3
1000	PILOT LED4
1001 to 1111	OFF (Reserved)

Write Pointer, FIFO_WR_PTR[4:0]

FIFO_WR_PTR[4:0] points to the FIFO location where the next sample will be written. This pointer advances for each sample pushed on to the FIFO by the internal conversion process. The write pointer is a 5-bit counter and will wrap around to count 0x00 on the next sample after count 0x1F.

Overflow Counter, OVF_COUNTER[4:0]

OVF_COUNTER[4:0] logs the number of samples lost if the FIFO is not read in a timely fashion. This counter holds at count value 0x1F. When a complete sample is popped from the FIFO (when the read pointer advances), the OVF_COUNTER is reset to zero. This counter is essentially a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred.

Read Pointer, FIFO_RD_PTR[4:0]

FIFO_RD_PTR[4:0] points to the location from where the next sample from the FIFO will be read through the interface. This advances each time a sample is read from the FIFO. The read pointer can be both read and written to. This allows a sample to be reread from the FIFO if it has not already been overwritten. The read pointer is updated from a 5-bit counter and will wrap around to count 0x00 from count 0x1F.

FIFO Data, FIFO_DATA[7:0]

FIFO_DATA[7:0] is a read-only register used to retrieve data from the FIFO. The format and data type of the data stored in the FIFO is determined by the LED Sequence register. Readout from the FIFO follows a progression defined by LED Sequence register as well. This configuration is best illustrated by a few examples.

Assume it is desired to perform a measurement with three LEDs sequentially as shown in Figure 2. The time for the LED to settle (t_{LED_STLNG}) is 20µs. To perform this measurement, configure the following registers:

Mode Configuration field

MODE[1:0] = 0x3 (FLEX LED Mode)

LED Sequence field

LEDC1[3:0] = 0x1 (LED1)

LEDC2[3:0] = 0x2 (LED2)

LEDC3[3:0] = 0x3 (LED3)

LEDC4[3:0] = 0x0 (OFF)

Configuration

ADC_RGE[1:0] (Gain Range Control)

SR[3:0] (Sample Rate Control)

LED_PW[1:0] (Integration Time)

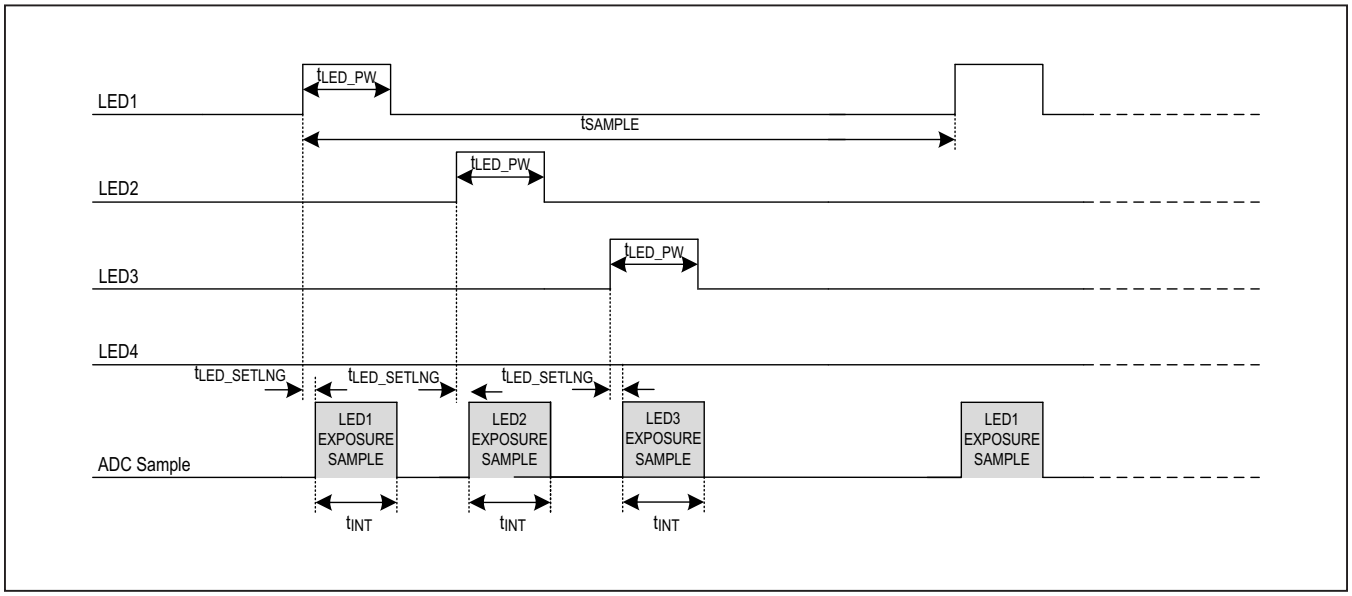


Figure 2. LED Sequence Timing Diagram with 3 Data Items Sampling.

LED Pulse Amplitude

LED1_PA[7:0] (LED1 Current Pulse Amplitude)

LED2_PA[7:0] (LED2 Current Pulse Amplitude)

LED3_PA[7:0] (LED3 Current Pulse Amplitude)

When done so the sample sequence and the data format in the FIFO will follow the following time/location sequence.

LED1 sample 1

LED2 sample 1

LED3 sample 1

LED1 sample 2

LED2 sample 2

LED3 sample 2

.

.

.

LED1 sample n

LED2 sample n

LED3 sample n

where:

LED1 sample x = ADC count exposure data from LED1 for the sample x

LED2 sample x = ADC count exposure data from LED2 for the sample x

LED3 sample x = ADC count exposure data from LED3 for the sample x

n is the number of samples in the FIFO, which can be up to 32 samples.

The number of active data samples in the FIFO is directly readable by subtracting the FIFO_RD_PTR[4:0] from the FIFO_WR_PTR[4:0], and taking wrap around of the pointers into consideration. It is typically controlled in the system by generating an interrupt on the INTB line when the FIFO reaches a watermark level computed from the FIFO_A_FULL[3:0] field in the FIFO Configuration register (0x08). In this case when the active data samples in the FIFO reach a level given by 32 - FIFO_A_FULL[3:0] an A_FULL interrupt is generated.

To calculate the number of active samples when the INTB signal is asserted, execute the following pseudo-code:

```
read the OVF_COUNTER register
read the FIFO_WR_PTR register
read the FIFO_RD_PTR register
if (OVF_COUNTER == 0) then //no overflow occurred
    if (FIFO_WR_PTR > FIFO_RD_PTR) then
        NUM_AVAILABLE_SAMPLES = FIFO_WR_PTR – FIFO_RD_PTR
    else
        NUM_AVAILABLE_SAMPLES = FIFO_WR_PTR + 32 - FIFO_RD_PTR
    endif
else
    NUM_AVAILABLE_SAMPLES = 32 // overflow occurred and data has been lost
endif
```

Optical data, whether ambient corrected LED exposure, ambient corrected proximity or direct ambient sampled data is as shown in the Table 3. The ADC data is left-justified at FIFO_DATA[18] and the MSBs (FIFO_DATA[23:18]) are don't care and should be masked as shown in Table 3. In other words, the MSB bit of the ADC data is always in the bit 18 position.

Table 3. Integration Pulse Width, Resulting ADC Resolution and FIFO Data Format

	FIFO DATA FORMAT (FIFO_DATA[23:0])																							
ADC Res	**ADC Value**																							
	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
19-bits	X	X	X	X	X	O18	O17	O16	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

FIFO Almost Full (Watermark)

The FIFO_A_FULL[3:0] register in the FIFO_Configuration register (0x08) determines when the A_FULL bit in the Interrupt_Status 1 register (0x00) gets asserted. The FIFO is almost full when it has 32 minus FIFO_A_FULL[3:0] samples. Then, if A_FULL_EN mask bit in the Interrupt_Enable 1 register (0x02) is set, the A_FULL bit in the Interrupt Status 1 will be set and routed to the INTB pin on the MAX86916 interface. This condition prompts the Application Processor to read samples from the FIFO before it gets filled. The A_FULL bit is cleared and INTB is deasserted when the status register is read.

When the Application Processor receives an interrupt, there are at least 32 minus FIFO_A_FULL[3:0] samples available in the FIFO. It is not necessary to read the FIFO_WR_PTR and FIFO_RD_PTR registers. The Application Processor may read all the available samples in the FIFO, or only a portion of it. At high sample rates, it is recommended that only a portion of the available samples are read on an A_FULL interrupt, to ensure that FIFO reading does not happen when the next sample conversion is in progress. The remaining samples will be read on the next interrupt.

If the A_FULL interrupt is not enabled, the Application Processor has to read the FIFO in polling mode. In this mode the Application Processor has to read the FIFO_WR_PTR and FIFO_RD_PTR registers to calculate the number of samples available in the FIFO, and then decide how many samples to read. However, polling mode is not recommended, because in this mode an interface transaction will inevitably overlap an optical sample, potentially adding noise to the optical data. Because of this concern, the interface transaction should occur during the dead time between optical samples to avoid adding additional noise.

FIFO_RO (FIFO Roll Over)

The FIFO_RO bit in the FIFO_Configuration register (0x08) determines whether samples get pushed on to the FIFO when it is full. If push is enabled when FIFO is full, old samples are lost. If FIFO_RO is not set, the new sample is dropped and the FIFO is not updated.

I²C/SMBus Compatible Serial Interface

The MAX86916 features an I²C/SMBus compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX86916 and the master at clock rates up to 400kHz.

The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX86916 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX86916 is 8-bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX86916 transmits the proper slave address followed by a series of nine SCL pulses. The MAX86916 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor is required on SDA. SCL operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX86916 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Detailed I²C Timing Diagram

The detailed timing diagram of various electrical characteristics is shown in Figure 3.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the MAX86916. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

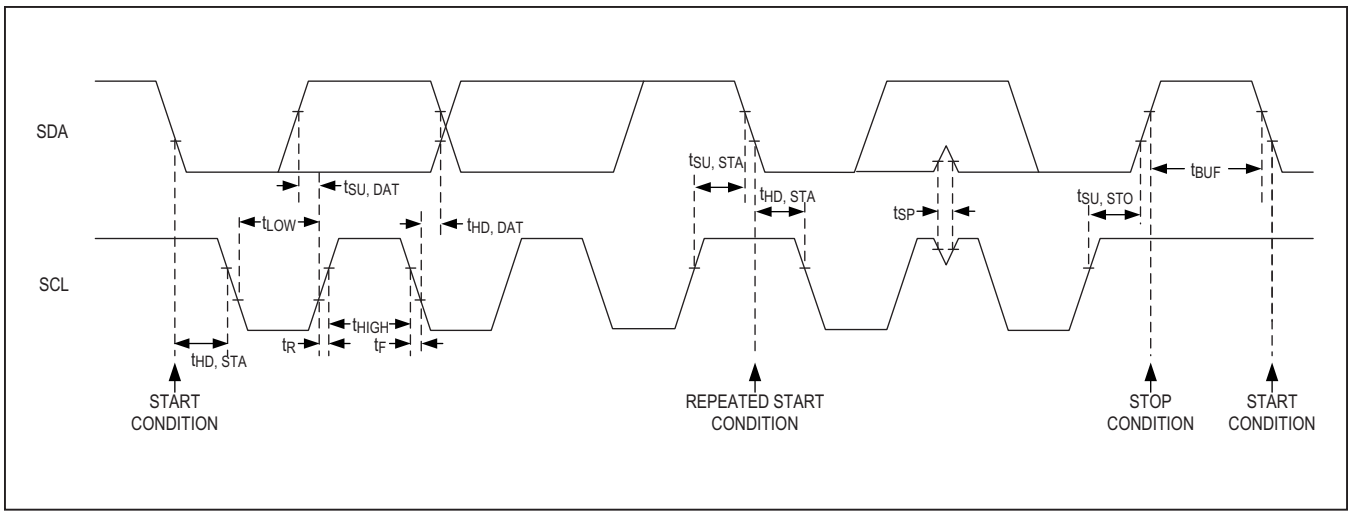


Figure 3. Detailed I²C Timing Diagram

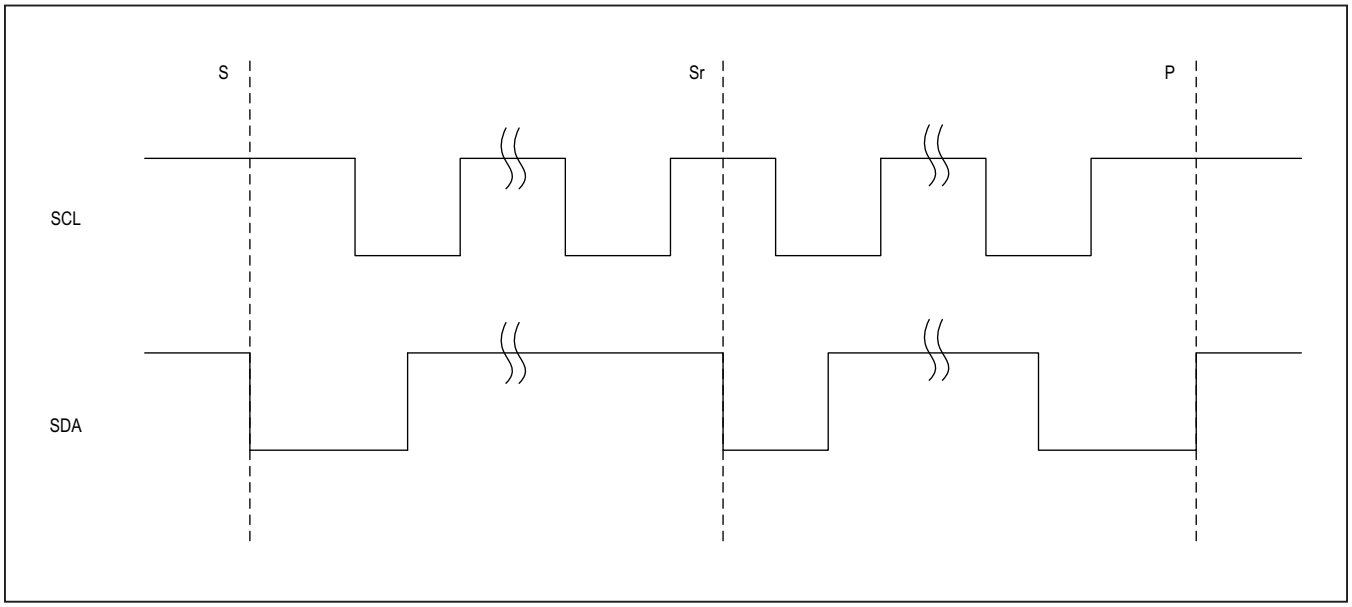


Figure 4: I²C START, STOP, and REPEATED START Conditions

Early STOP Conditions

The MAX86916 recognizes a STOP condition at any point during data transmission unless the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX86916 the seven most significant bits are 0b1010111. For read mode, set the read/write bit to 1. For write mode, set the read/write bit to 0. The address is the first byte of information sent to the IC after the START condition.

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX86916 uses to handshake receipt each byte of data when in write mode (Figure 5). The MAX86916 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX86916 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX86916, followed by a STOP condition.

I²C Write Data Format

A write to the MAX86916 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 6 illustrates the proper frame format for writing one byte of data to the MAX86916. Figure 7 illustrates the frame format for writing n-bytes of data to the MAX86916.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX86916. The MAX86916 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX86916's internal register address pointer. The pointer tells the MAX86916 where to write the next byte of data. An acknowledge pulse is sent by the MAX86916 upon receipt of the address pointer data.

The third byte sent to the MAX86916 contains the data that will be written to the chosen register. An acknowledge pulse from the MAX86916 signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. The auto_increment feature is disabled when there is an attempt to write to the FIFO_DATA register.

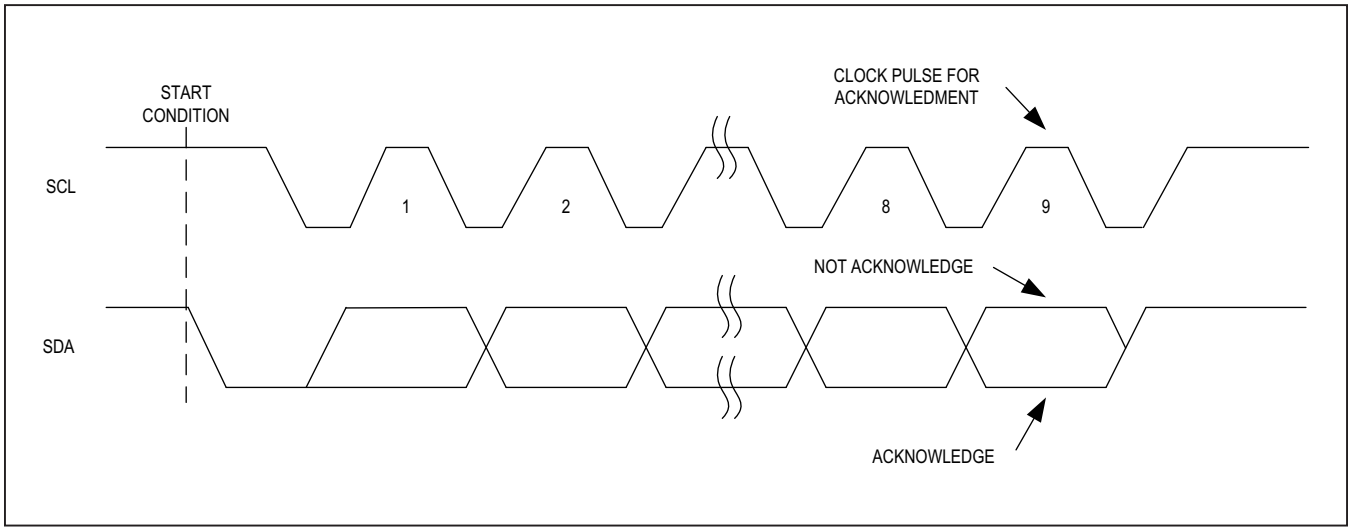


Figure 5. I²C Acknowledge Bit

I²C Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX86916 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX86916 will be the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. The auto_increment feature is disabled when there is an attempt to read from the FIFO_DATA register. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX86916 slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX86916 then transmits the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 8 illustrates the frame format for reading one byte from the MAX86916. Figure 9 illustrates the frame format for reading multiple bytes from the MAX86916.

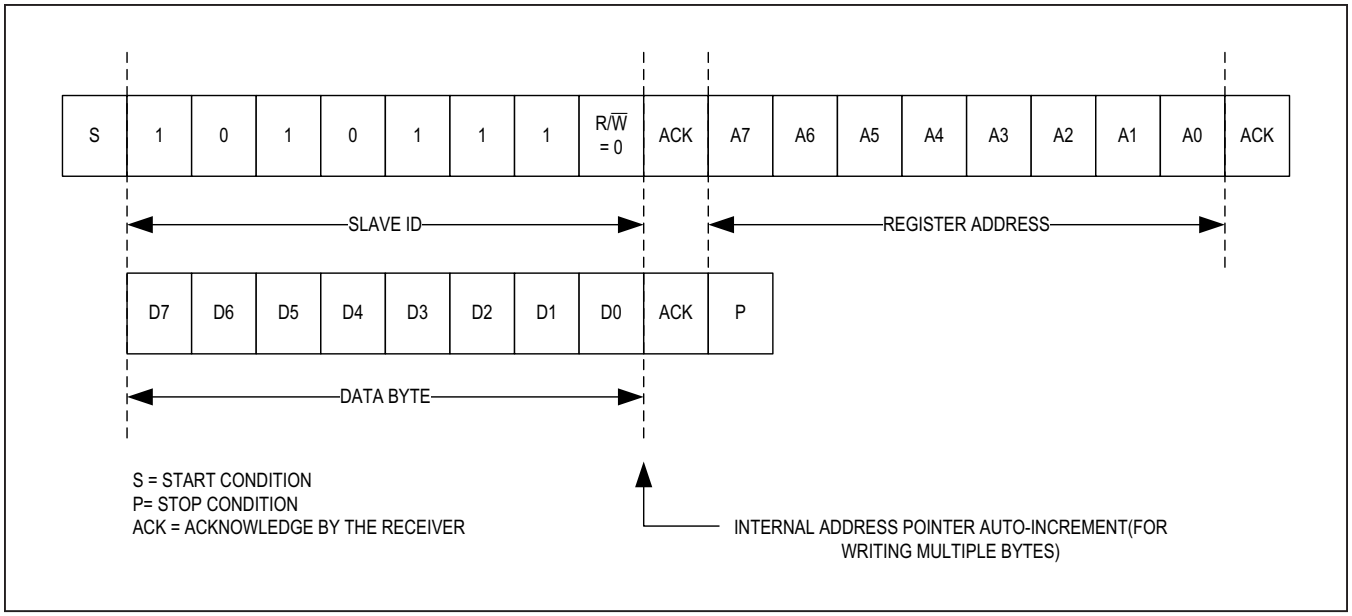


Figure 6. I²C Single Byte Write Transaction

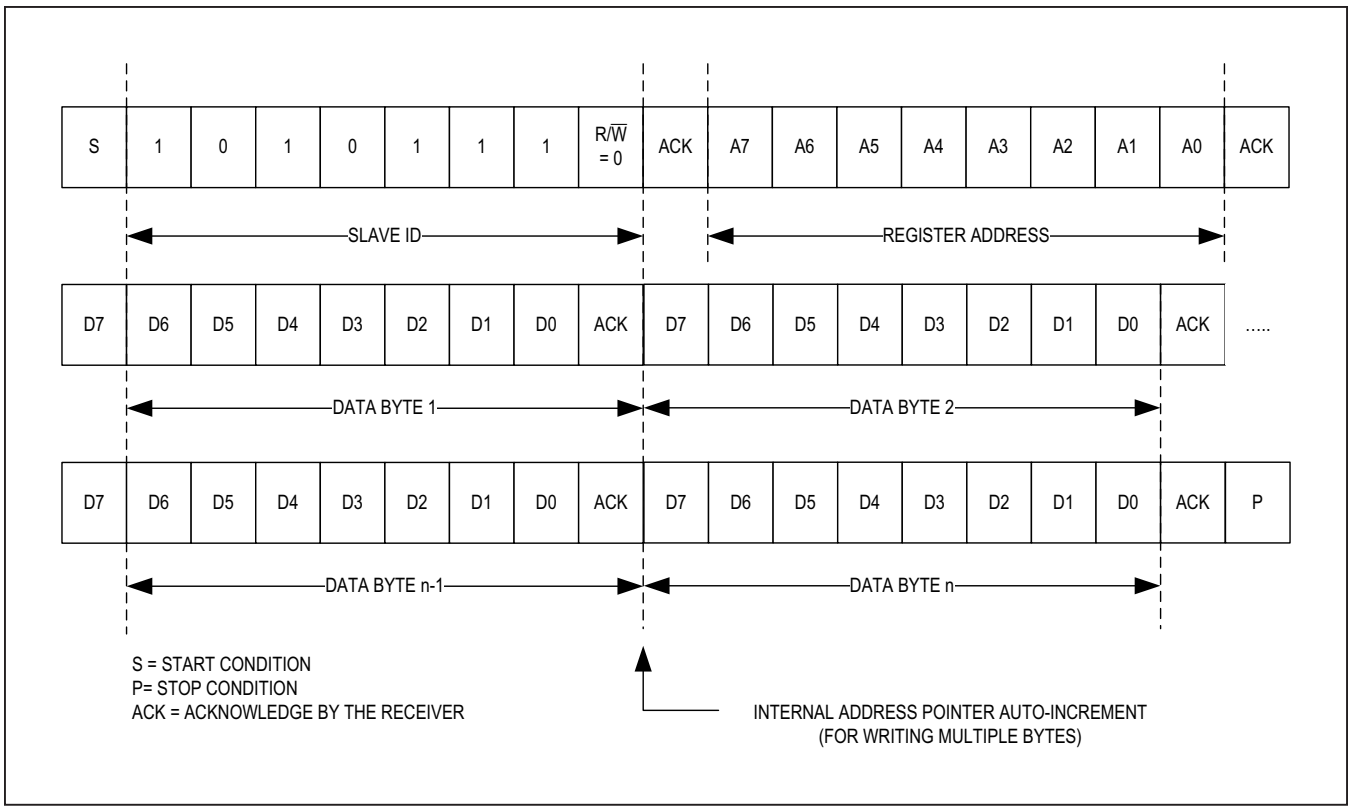


Figure 7. I²C Multi-Byte Write Transaction

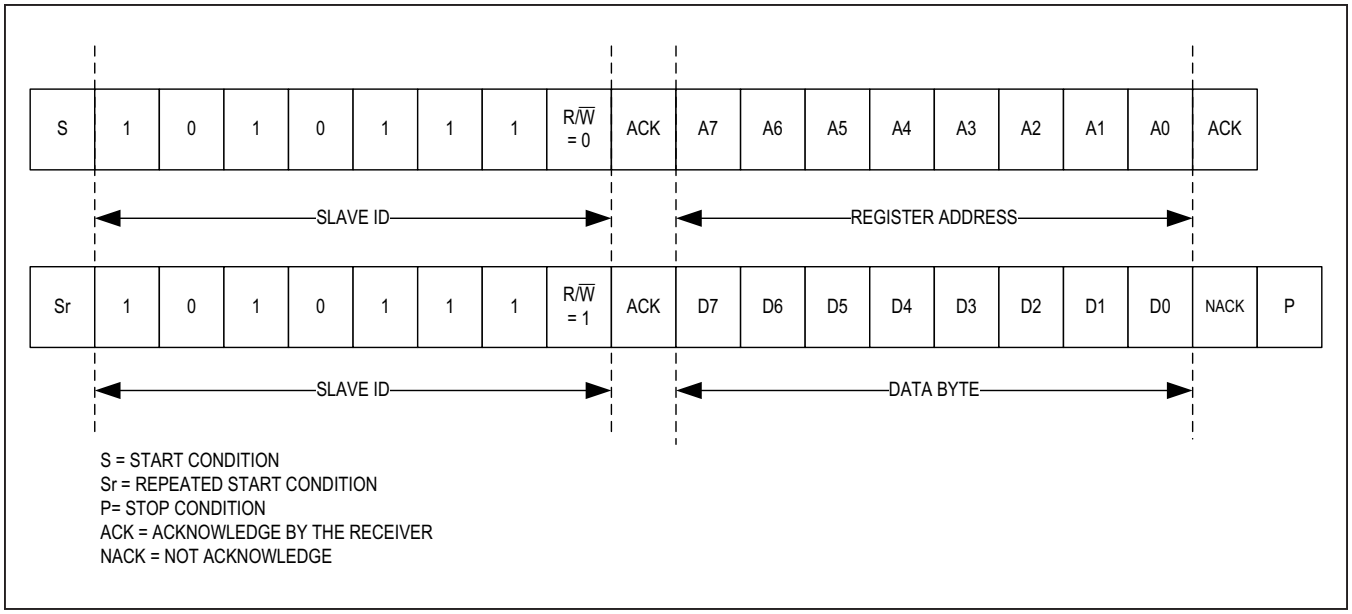


Figure 8. I²C Single Byte Read Transaction

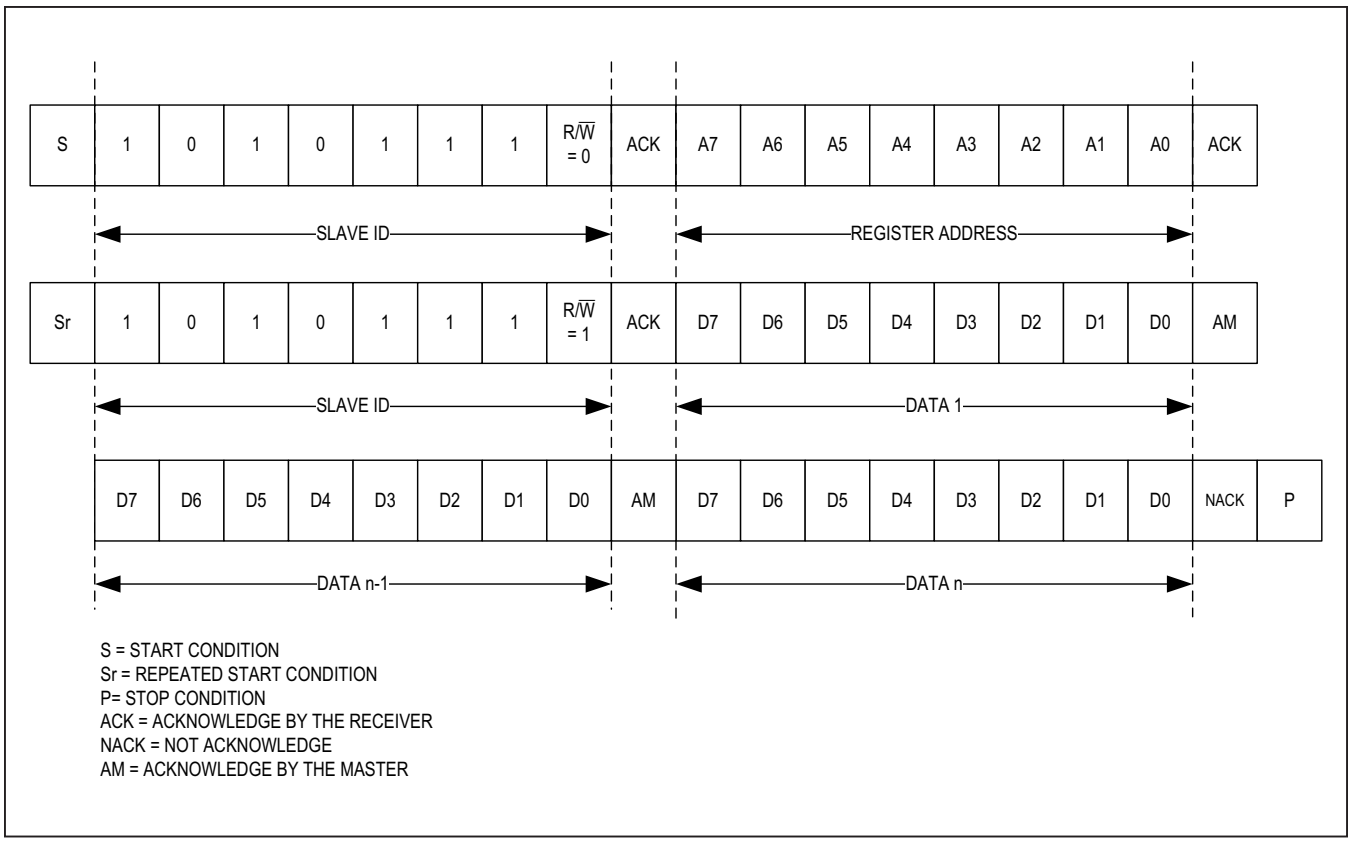


Figure 9. I²C Multi-Byte Read Transaction

Register Map

User Register Map

ADDRESS	NAME	MSB							LSB
STATUS REGISTERS									
0x00	Interrupt Status 1[7:0]	A_FULL	SMP_RDY	ALC_OVF	PROX_INT	–	–	–	PWR_RDY
0x01	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x02	Interrupt Enable 1[7:0]	A_FULL_EN	SMP_RDY_EN	ALC_OVF_EN	PROX_INT_EN	–	–	–	–
0x03	RESERVED[7:0]	–	–	–	–	–	–	–	–
FIFO REGISTERS									
0x04	FIFO Write Pointer[7:0]	–	–	–	FIFO_WR_PTR[4:0]				
0x05	Over Flow Counter[7:0]	–	–	–	OVF_COUNTER[4:0]				
0x06	FIFO Read Pointer[7:0]	–	–	–	FIFO_RD_PTR[4:0]				
0x07	FIFO Data Register[7:0]	FIFO_DATA[7:0]							
CONFIGURATION									
0x08	FIFO Configuration[7:0]	SMP_AVE[2:0]			FIFO_RO	FIFO_A_FULL[3:0]			
0x09	Mode Configuration 1[7:0]	SHUT-DOWN	RESET	–	RE-SERVED	RE-SERVED	AMB_LIGHT_DET	MODE[1:0]	
0x0A	Mode Configuration 2[7:0]	RE-SERVED	ADC_RGE[1:0]		SR[2:0]			LED_PW[1:0]	
0x0B	RESERVED[7:0]	–	–	–	–	–	–	–	–
LED PULSE AMPLITUDE									
0x0C	LED1 PA[7:0]	LED1_PA[7:0]							
0x0D	LED2 PA[7:0]	LED2_PA[7:0]							
0x0E	LED3 PA[7:0]	LED3_PA[7:0]							
0x0F	LED4 PA[7:0]	LED4_PA[7:0]							
0x11	LED Range[7:0]	LED4_RGE[1:0]		LED3_RGE[1:0]		LED2_RGE[1:0]		LED1_RGE[1:0]	
0x12	Pilot PA[7:0]	PILOT_PA[7:0]							
LED SEQUENCE CONTROL									
0x13	LED Sequence Register 1[7:0]	LEDC2[3:0]				LEDC1[3:0]			
0x14	LED Sequence Register 2[7:0]	LEDC4[3:0]				LEDC3[3:0]			

Register Map (continued)

ADDRESS	NAME	MSB							LSB
RESERVED									
0x1F	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x20	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x21	RESERVED[7:0]	–	–	–	–	–	–	–	–
RESERVED									
0x22	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x23	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x24	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x25	RESERVED[7:0]	–	–	–	–	–	–	–	–
CROSSTALK DAC									
0x26	DAC1 Crosstalk Code[7:0]	–	–	–	XTALK_DAC1[4:0]				
0x27	DAC2 Crosstalk Code[7:0]	–	–	–	XTALK_DAC2[4:0]				
0x28	DAC3 Crosstalk Code[7:0]	–	–	–	XTALK_DAC3[4:0]				
0x29	DAC4 Crosstalk Code[7:0]	–	–	–	XTALK_DAC4[4:0]				
PROXIMITY MODE									
0x30	Proximity Interrrupt Threshold[7:0]	PROX_INT_THRESH[7:0]							
LED CONNECTIVITY TEST									
0x31	LED Comparator Enable[7:0]	LED_ TEST_EN4	LED_ TEST_EN3	LED_ TEST_EN2	LED_ TEST_EN1	–	–	–	COMP
0x32	LED Comparator Status[7:0]					COMP_ OUT4	COMP_ OUT3	COMP_ OUT2	COMP_ OUT1
RESERVED									
0x51	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x52	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x53	RESERVED[7:0]	–	–	–	–	–	–	–	–
0x54	RESERVED[7:0]	–	–	–	–	–	–	–	–
PART ID									
0xFE	Revision ID[7:0]	REV_ID[7:0]							
0xFF	Part ID[7:0]	PART_ID[7:0]							

Register Details

Interrupt Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	SMP_RDY	ALC_OVF	PROX_INT	–	–	–	PWR_RDY
Reset	0x0	0x0	0x0	0x0	–	–	–	0x1
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	–	Read Only

A_FULL

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that the FIFO buffer will overflow the threshold set by FIFO_A_FULL[3:0] on the next sample. The interrupt is cleared by reading the Interrupt Status 1 register (0x00).

SMP_RDY

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	This interrupt triggers when there is a new sample in the data FIFO. The interrupt is cleared by reading the Interrupt Status 1 register (0x00), or by reading the FIFO_DATA register.

ALC_OVF

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	This interrupt triggers when the ambient light cancellation function of the photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC. The interrupt is cleared by reading the Interrupt Status 1 register (0x00).

PROX_INT

See *Proximity Function* for more details.

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that the proximity threshold has been crossed when in proximity mode. If PROX_INT is masked by setting PROX_INT_EN to 0, then the proximity mode is disabled and the selected operating MODE begins immediately. The interrupt is cleared by reading the Interrupt Status 1 register (0x00).

PWR_RDY

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that VDD went below the UVLO (< 1.55V, typ.) threshold. This bit is not set to 1 by a soft reset. The interrupt is cleared by reading the Interrupt Status 1 register (0x00).

Interrupt Enable 1 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN	SMP_RDY_EN	ALC_OVF_EN	PROX_INT_EN	–	–	–	–
Reset	0x0	0x0	0x0	0x0	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

A_FULL_EN

VALUE	ENUMERATION	DECODE
0	OFF	A_FULL interrupt is disabled
1	ON	A_FULL interrupt is enabled

SMP_RDY_EN

VALUE	ENUMERATION	DECODE
0	OFF	SMP_RDY interrupt is disabled
1	ON	SMP_RDY interrupt is enabled.

ALC_OVF_EN

VALUE	ENUMERATION	DECODE
0	OFF	ALC_OVF interrupt is disabled
1	ON	ALC_OVF interrupt is enabled

PROX_INT_EN

When the sensor is initiated with PROX_INT_EN = 1, the LED1 is turned on in proximity mode with a drive current set by the PILOT_PA register. When an object is detected by exceeding the Proximity Mode Threshold (set in the PROX_INT_THRESH register), PROX_INT interrupt is asserted and the part transitions automatically to the programmed configuration set is MODE.

See *Proximity Function* for more details.

VALUE	ENUMERATION	DECODE
0	OFF	PROX_INT interrupt is disabled
1	ON	PROX_INT interrupt is enabled

FIFO Write Pointer (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FIFO_WR_PTR[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Read Only				

FIFO_WR_PTR

This points to the location where the next sample will be written. This pointer advances for each sample pushed on to the FIFO.

See *FIFO Configuration* for more details.

Overflow Counter (0x05)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	OVF_COUNTER[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Read Only				

OVF_COUNTER

When FIFO is full any new samples will result in new or old samples getting lost depending on FIFO_RO. OVF_COUNTER counts the number of samples lost. It saturates at 0x1F. It gets reset to 0 when a sample is read from the FIFO.

See *FIFO Configuration* for more details.

FIFO Read Pointer (0x06)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FIFO_RD_PTR[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

FIFO_RD_PTR

The FIFO Read Pointer points to the location from where the processor gets the next sample from the FIFO via the I^2C interface. This advances each time a sample is popped from the FIFO. The processor may also write to this pointer after reading the samples. This allows rereading (or retrying) samples from the FIFO.

See *FIFO Configuration* for more details.

FIFO Data Register (0x07)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_DATA

This is a read-only register and is used to get data from the FIFO.

See *FIFO Configuration* for more details.

FIFO Configuration (0x08)

BIT	7	6	5	4	3	2	1	0
Field	SMP_AVE[2:0]			FIFO_RO	FIFO_A_FULL[3:0]			
Reset	0x0			0x0	0xF			
Access Type	Write, Read			Write, Read	Write, Read			

SMP_AVE

Adjacent samples (of each individual LED) can be internally averaged to reduce the amount of data throughput. Each LED channel will be averaged individually and output sequentially as programmed in the LED Seruence Registers.

These bits set the number of samples that are averaged on chip before being written to the FIFO. The effective output sample rate is the sample rate programmed in SR divided by the Sample Average value based on the table below:

SMP_AVE[2:0]	SAMPLE AVERAGE
000	1
001	2
010	4
011	8
100	16
101	32
110	32
111	32

FIFO_RO

Push enable when FIFO is full:

This bit controls the behavior of the FIFO when the FIFO becomes completely filled with data.

Push to FIFO is enabled when FIFO is full if FIFO_RO = 1. In this mode old samples are overwritten. FIFO_WR_PTR increments for each sample. FIFO_RD_PTR also increments for each sample pushed to the FIFO.

Push to FIFO is disabled when FIFO is full if FIFO_RO = 0. In this mode old samples are not overwritten and new samples are discarded . FIFO_WR_PTR and FIFO_RD_PTR do not increment for each sample after the FIFO is full.

When the device is in proximity mode, push to FIFO is enabled independent of FIFO_RO setting. The FIFO is flushed when the PROX_INT is triggered.

See *Proximity Function* for more details.

VALUE	ENUMERATION	DECODE
0	OFF	The FIFO stops on full.
1	ON	The FIFO automatically rolls over on full.

FIFO_A_FULL

These bits indicate how many unread samples are in the FIFO when the interrupt is asserted. For example, if set to 0xF, the interrupt triggers when there are 17 data samples in the FIFO (15 empty spaces lefts).

See FIFO Configuration for more details.

FIFO_A_ FULL[3:0]	FREE SPACE AT INTERRUPT	# OF SAMPLES IN FIFO
0000	0	32
0001	1	31
0010	2	30
0011	3	29
—	—	—
1110	14	18
1111	15	17

Mode Configuration 1 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	SHUTDOWN	RESET	–	RESERVED	RESERVED	AMB_LIGHT_DET	MODE[1:0]	
Reset	0x0	0x0	–	0x0	0x0	0x0	0x0	
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	

SHUTDOWN

Shutdown Control

VALUE	ENUMERATION	DECODE
0x0	0	Normal Operation
0x1	1	The part can be put into a power-save mode by writing a ‘1’ to this bit. While in this mode all configuration and control registers remain accessible and retain their data. All interrupts are cleared. In this mode the oscillator is shutdown and the part draws minimum current.

RESET

Software Reset

VALUE	ENUMERATION	DECODE
0x0	0	Normal operation
0x1	1	The part under-goes a forced power-on-reset sequence. All the registers, except PWR_RDY, are reset to their power-on-reset state. The RESET bit then automatically resets to 0 after the reset sequence is completed.

AMB_LIGHT_DET

Ambient Light Detection Mode Enable. ALC and digital filter are disabled when AMB_LIGHT_DET = 1.

VALUE	ENUMERATION	DECODE
0x0	0	Normal Operation
0x1	1	Ambient Light Detection Mode disabled.

MODE

These bits set the operating mode

MODE[1:0]	MODE
00	Disabled
01	LED1 Enabled. Only one ADC conversion for LED1 (IR LED)
10	LED1 and LED2 Enabled. Two ADC conversions sequencitally for LED1 (IR LED) and LED2 (RED LED)
11	Flex LED Mode. Number of ADC conversions and the LED types are programmed in the LED Sequence Registers.

Mode Configuration 2 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	ADC_RGE[1:0]		SR[2:0]			LED_PW[1:0]	
Reset	0x0	0x0		0x0			0x0	
Access Type	Write, Read	Write, Read		Write, Read			Write, Read	

ADC_RGE

These bits set the ADC range of the sensor as shown in the table below.

ADC_ RGE[1:0]	LSB (PA)	FULL SCALE (NA)
00	7.81	4096
01	15.63	8192
10	31.25	16384
11	62.50	32768

SR

These bits set the sampling rate of the optical sensor as shown in the table below.

SR[2:0]	SAMPLE PER SECOND
0	50
1	100
2	200
3	400
4	800
5	1000
6	1600
7	3200

Maximum Sample rates (Hz) supported for all the Pulse Widths and Number of Conversions:

NUMBER OF LEDS FIRING PER SAMPLE	LED_PW[1:0]			
	0x0	0x1	0x2	0x3
1	3200	1600	1000	400
2	1600	1000	400	200
3	1000	400	400	200
4	800	400	200	100

LED_PW

These bits set the pulse width of the LED drivers and the integration time of ADC as shown in the table below.

LED_PW[1:0]	PULSE WIDTH [µs]	INTEGRATION TIME [µs]	RESOLUTION [BITS]
00	70	50	19
01	120	100	19
10	220	200	19
11	420	400	19

LED1 PA (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	LED1_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED1_PA

These bits set the nominal current pulse amplitude of LEDx (x = 1 to 4) as shown in the table below.

LEDX_RGE[1:0]	0X0	0X1	0X2	0X3
LEDx_PA[7:0], (x = 1 to 4), PILOT_PA	LED CURRENT[mA]	LED CURRENT[mA]	LED CURRENT[mA]	LED CURRENT[mA]
0000 0000	0	0	0	0
0000 0001	0.2	0.4	0.6	0.8
0000 0010	0.4	0.8	1.2	1.6
0000 0011	0.6	1.2	1.8	2.4
.....				
1111 1100	49.8	99.6	149.4	199.2
1111 1101	50	100	150	200
1111 1110	50.2	100.4	150.6	200.8
1111 1111	50.4	100.8	151.2	201.6
LSB	0.2	0.4	0.6	0.8

LED2 PA (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	LED2_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED2_PA

See description under LED1_PA.

LED3 PA (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	LED3_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED3_PA

See description under LED1_PA.

LED4 PA (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	LED4_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED4_PA

See description under LED1_PA.

LED Range (0x11)

BIT	7	6	5	4	3	2	1	0
Field	LED4_RGE[1:0]		LED3_RGE[1:0]		LED2_RGE[1:0]		LED1_RGE[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

LED4_RGE

Range selection of the LED current. Please refer to LED1_PA[7:0] for more details.

LEDX_RGE[1:0] (X = 1 TO 4)	LED CURRENT [mA]
00	50
01	100
10	150
11	200

LED3_RGE

See description under LED4_RGE.

LED2_RGE

See description under LED4_RGE.

LED1_RGE

See description under LED4_RGE.

Pilot PA (0x12)

BIT	7	6	5	4	3	2	1	0
Field	PILOT_PA[7:0]							
Reset	0x0							
Access Type	Write, Read							

PILOT_PA

PILOT_PA is used for driving the LED when PILOT_LED1-4 is configured in LEDCx register.

See description under LED1_PA.

LED Sequence Register 1 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	LEDC2[3:0]				LEDC1[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

LEDC2

When Mode[1:0] = 0x3 the LED Sequence Registers LEDC1, LEDC2, LEDC3, and LEDC4 control the turn on and sequencing of the LED drivers. For settings 0x1 to 0x4, the LEDx_PA setting for the enabled LED driver is used, but for settings 0x5 to 0x8 the PA setting for the PILOT_PA is used. PILOT LED is generally used by setting a different PA settings for all LED channels. It is generally used with lower PA settings for a lower power mode.

The LED Sequence Registers also sets the data type of element x of the sample in the FIFO.

See *FIFO Configuration* for more details.

LEDCX[3:0], X = 1, 2, 3, 4	LED
0000	OFF
0001	LED1
0010	LED2
0011	LED3
0100	LED4
0101	PILOT LED1
0110	PILOT LED2
0111	PILOT LED3
1000	PILOT LED4
1001 to 1111	OFF (Reserved)

LEDC1

See description under LEDC2.

LED Sequence Register 2 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	LEDC4[3:0]				LEDC3[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

LEDC4

See description under LEDC2.

LEDC3

See description under LEDC2.

DAC1 Crosstalk Code (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	XTALK_DAC1[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

XTALK_DAC1

XTALK_DACx[4:0] (x = 1 to 4) sets the crosstalk cancellation DAC code used in ADC. The DAC code is used to subtract a DC component of the received optical signal at the photodetector that is coherent with the LED pulse. The intent of this feature is to cancel out the crosstalk caused by the system level optical design, especially when high reflective or translucent cover glass is used. The final optical system design will need to be characterized to set the code for XTALK_DACx. The FULL RANGE of the DAC code is dependent of setting used in ADC_RGE[1:0], as shown in the following table.

Crosstalk cancellation is disabled when XTALK_DACx[4:0] (x = 1 to 4) code is 0.

	XTALK_DACX[4:0] (X = 1 TO 4)	
ADC_RGE[1:0]	LSB (nA)	FULL SCALE (nA)
00	64	1984
01	128	3968
10	256	7936
11	512	15872

DAC2 Crosstalk Code (0x27)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	XTALK_DAC2[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

XTALK_DAC2

See description under XTALK_DAC1.

DAC3 Crosstalk Code (0x28)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	XTALK_DAC3[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

XTALK_DAC3

See description under XTALK_DAC1.

DAC4 Crosstalk Code (0x29)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	XTALK_DAC4[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

XTALK_DAC4

See description under XTALK_DAC1.

Proximity Interrrupt Threshold (0x30)

BIT	7	6	5	4	3	2	1	0
Field	PROX_INT_THRESH[7:0]							
Reset	0x0							
Access Type	Write, Read							

PROX_INT_THRESH

This register sets the LED1 ADC count value that will trigger the transition between proximity mode to normal mode. The threshold is defined as the 8 MSB bits of the ADC count. For example, if PROX_INT_THRESH[7:0] = 0x01, then an ADC value of 2048 (decimal) or higher triggers the PROX interrupt. If PROX_INT_THRESH[7:0] = 0xFF, then only a saturated ADC triggers the interrupt.

Please see the *Proximity Function* section in the detailed description for more details on the operation of proximity mode.

LED Comparator Enable (0x31)

BIT	7	6	5	4	3	2	1	0
Field	LED_TEST_EN4	LED_TEST_EN3	LED_TEST_EN2	LED_TEST_EN1	–	–	–	COMP
Reset	0x0	0x0	0x0	0x0	–	–	–	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	Write, Read

LED_TEST_EN4

When COMP[0] = 0x1, this bit is dedicated to force LED4 enable to check LED4 failure. This test should check one LED driver at a time.

VALUE	ENUMERATION	DECODE
0	OFF	Disable LED4
1	ON	Enable LED4

LED_TEST_EN3

When COMP[0] = 0x1, this bit is dedicated to force LED3 enable to check LED3 failure. This test should check one LED driver at a time.

VALUE	ENUMERATION	DECODE
0	OFF	Disable LED3
1	ON	Enable LED3

LED_TEST_EN2

When COMP[0] = 0x1, this bit is dedicated to force LED2 enable to check LED2 failure. This test should check one LED driver at a time.

VALUE	ENUMERATION	DECODE
0	OFF	Disable LED2
1	ON	Enable LED2

LED_TEST_EN1

When COMP[0] = 0x1, this bit is dedicated to force LED1 enable to check LED1 failure. This test should check one LED driver at a time.

VALUE	ENUMERATION	DECODE
0	OFF	Disable LED1
1	ON	Enable LED1

COMP

This bit enables LED comparator to check LEDx failure.

VALUE	ENUMERATION	DECODE
0	OFF	Disable comparator
1	ON	Enable comparator

LED Comparator Status (0x32)

BIT		3	2	1	0
Field		COMP_ OUT4	COMP_ OUT3	COMP_ OUT2	COMP_ OUT1
Reset		0x0	0x0	0x0	0x0
Access Type		Read Only	Read Only	Read Only	Read Only

COMP_OUT4

This bit stores LED4's comparator output.

VALUE	ENUMERATION	DECODE
0		Normal
1		LED4 is open

COMP_OUT3

This bit stores LED3's comparator output.

VALUE	ENUMERATION	DECODE
0		Normal
1		LED3 is open

COMP_OUT2

This bit stores LED2's comparator output.

VALUE	ENUMERATION	DECODE
0		Normal
1		LED2 is open

COMP_OUT1

This bit stores LED1's comparator output.

VALUE	ENUMERATION	DECODE
0		Normal
1		LED1 is open.

Revision ID (0xFE)

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0xXX							
Access Type	Read Only							

REV_ID

This register stores revision ID which varies from 00(Hex) to FF(Hex). Contact Maxim Integrated for the revision ID number assigned for your product.

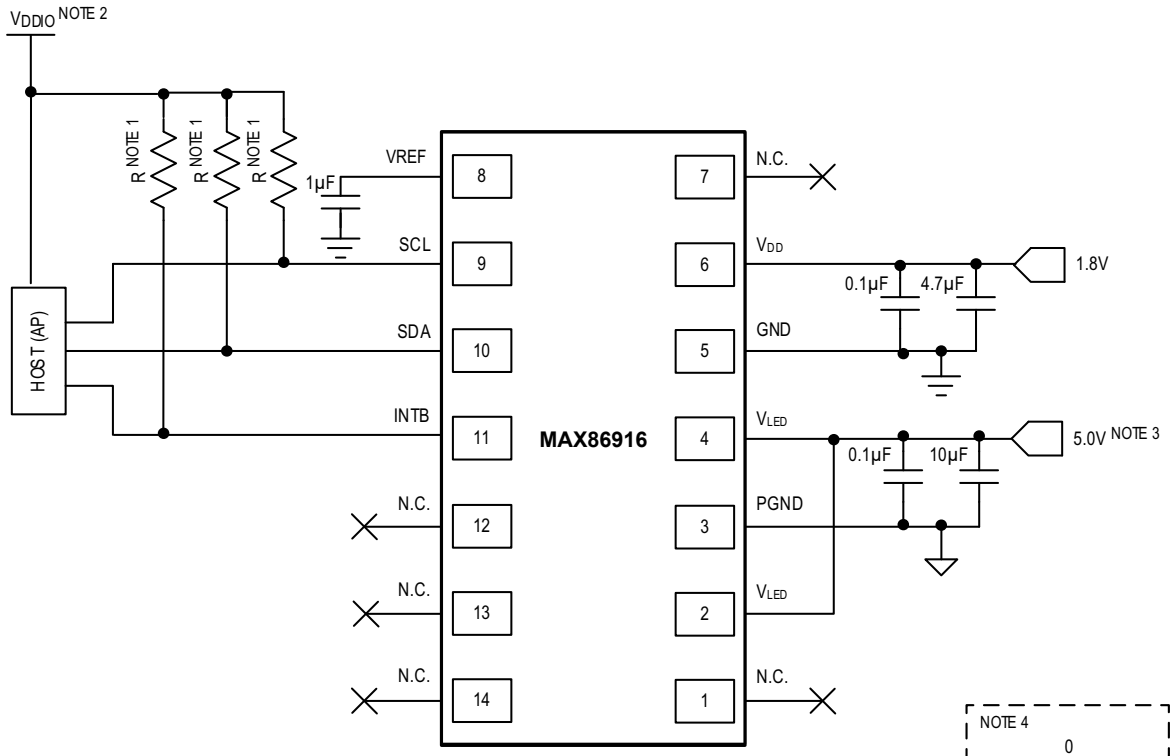
Part ID (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x2B							
Access Type	Read Only							

PART_ID

This register stores the Part identifier for the chip.

Typical Application Circuit



NOTE 1: THE VALUE OF SDA, SCL AND INTB PULLUP RESISTORS SHOULD BE BASED ON THE SYSTEM DESIGN.

NOTE 2: V_{DDIO} IS THE SYSTEM I/O VOLTAGE SUPPLY.

NOTE 3: V_{LED} IS THE LED POWER SUPPLY INPUT, IT SHOULD BE BASED ON THE SYSTEM APPLICATIONS AND LED CONFIGURATIONS USED.

NOTE 4: USE COMMON DESIGN PRACTICE TO ISOLATE NOISE COUPLING BETWEEN GND PLANES.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX86916EFD+T	-40°C to + 85°C	14-Lead OLGA

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/19	Initial release	—

