Keywords: Deglitching Techniques for High-Voltage R-2R DACs

APPLICATION NOTE 583

Deglitching Techniques for High-Voltage R-2R DACs

May 01, 2001

In an R-2R DAC design with supply voltages exceeding ±5V, large voltage glitches (up to 1.5V) can occur during the DAC's major-carry transitions. These glitches can propagate through the output buffer amplifier and appear at output. The slewing of the level shifters that control the top (V_{REF+}) and bottom (V_{REF-}) single-pole double-throw switches (S_0 to S_N) causes the glitches (**Figure 1**). If each switch of the "inverted" R-2R ladder were turned on and/or off instantaneously, glitch amplitudes at the DAC output (or input of the output buffer amplifier) would be small. However, switches do not switch instantaneously; in fact, to avoid crowbar current between outputs of the two reference buffers, the switches employ a break-before-make connection. The associated time delay can produce very large glitches during DAC code transitions that degrade the dynamic performance specification "glitch impulse energy."

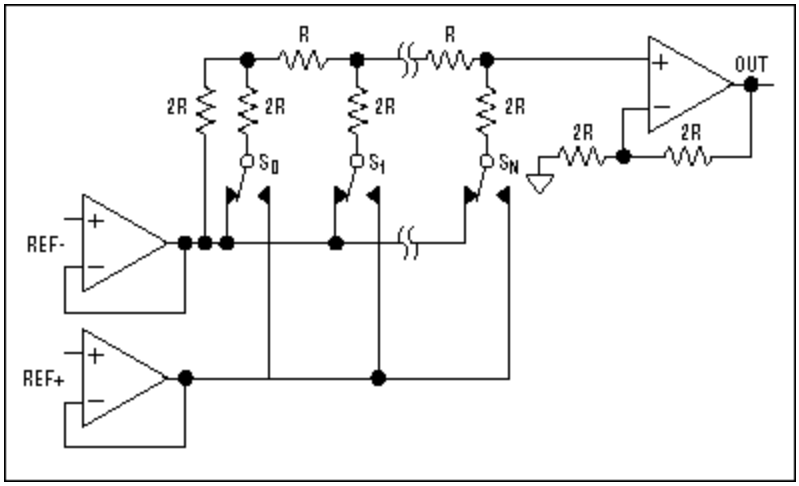

Figure 1. Simplified DAC circuit.

One way to reduce glitch energy is to connect a large capacitor between the DAC output and ground. The lowpass-filter combination of R_{DAC} and C reduces the amplitude of the glitch. However, to reduce the glitch significantly, the capacitance value must be large. Thus, this approach increases the DAC's settling time considerably.

Another deglitching technique is to use an external track/hold (T/H) amplifier following the DAC output. One advantage of this approach is that glitches at the DAC output can be eliminated completely (in principle). However, external one shot and deglitch timing control logic (in addition to the T/H amplifier)

are required. Thus, the interface between the DAC, the deglitch timing control circuit, and the T/H amplifier can be fairly cumbersome.

Integrating the T/H amplifier on the same chip as the DAC eliminates the cumbersome interface (**Figure 2**). The deglitch T/H amplifier is placed immediately following the buffered DAC output. Using this technique, a smart deglitch circuit has been developed that significantly reduces the digital-to-analog glitch impulse energy without increasing settling time.

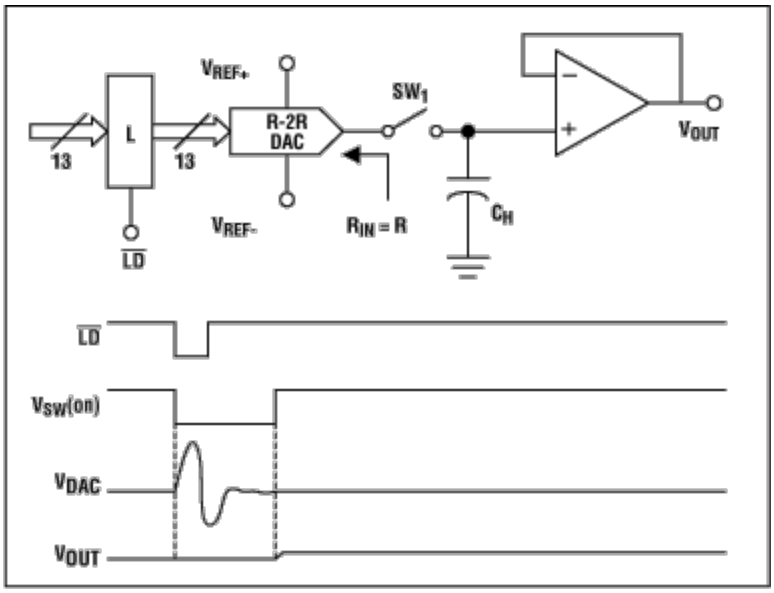

Figure 2. Integrated T/H deglitch architecture.

Smart DAC Deglitch Circuit

Because the glitch occurs right after a DAC is updated and disappears within the first few microseconds, if the DAC output and output buffer amplifier input are decoupled when the DAC is updated and stay decoupled until the glitch disappears, the glitch will not pass through the output buffer amplifier. As shown in Figure 2, this solution uses a T/H concept to eliminate glitches. Before the DAC is updated, switch SW1 is closed. The sampling capacitor samples the DC level of the previous DAC code. During a digital code transition, as the DAC is being updated the switch is opened and the capacitor (C_H) holds the DC level of the previous DAC code. The amplifier output is maintained at this DC level while the glitch occurs. After the glitch disappears, the switch closes again. Unlike the lowpass-filter technique discussed in the previous section, the value of the T/H capacitor can be much smaller, because this capacitor is used to hold the DC level of the previous DAC code, as opposed to reducing the amplitude of a glitch. Small glitches can still occur when the T/H switch is turned on or off due to charge sharing and injection, but the associated glitch amplitude is much smaller.

Implementation Techniques

Although combining the DAC output amplifier with a T/H appears obvious intuitively, this presents some design challenges during the actual implementation. For example, in some applications, a large DAC output swing is required. Therefore, the sampling switch (SW1) must operate with high-voltage potentials. This requirement limits the T/H implementation to a handful of processes having the required high breakdown voltage MOS switches. Another challenge is that the base current of the output amplifier's bipolar input pair can cause an offset voltage ($I_{BASE} \times R_{SW}$) across the switch (SW1). Finally,

charge injection and clock feedthrough are additional T/H circuit specifications that need to be considered.

An Improved Deglitch Circuit

With a unity-gain buffer amplifier following the DAC output, the sampling switch must have a high breakdown voltage. However, if the amplifier's gain is greater than one (n > 1), the required switch breakdown voltage will be reduced by a factor of n. This helps to relax the process requirements as they relate to the DAC and the switch. **Figure 3** shows the architecture of this circuit.

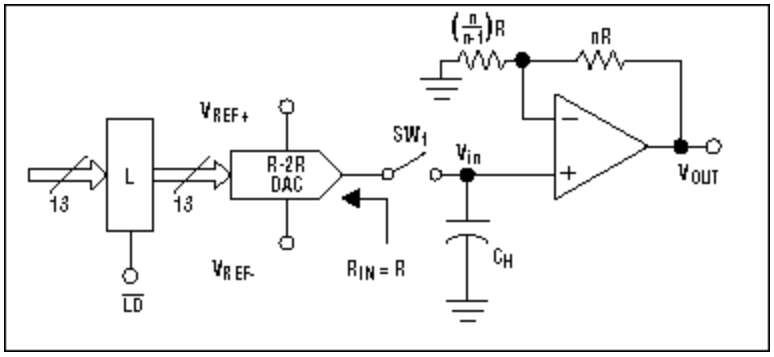

Figure 3. An improved deglitch circuit.

Designating V_{SW} as the switch voltage that controls the sampling switch, the process breakdown voltage ($V_{BREAKDOWN}$) limits the maximum value of V_{SW}. By setting $n>V_{out\ (MIN/MAX)}/V_{BREAKDOWN}$, the high-voltage concerns are mitigated.

Eliminating Offset Due to Non-zero Base Current

To eliminate the base current of the sampling switch, differential charge cancellation can be used, as shown in **Figure 4**.

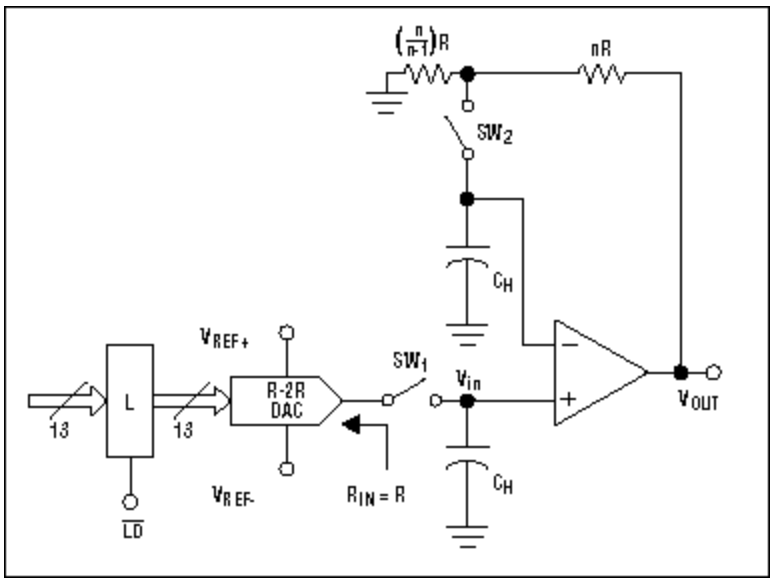

Figure 4. Differential charge cancellation.

SW_2 is equal to SW_1, and both see the same impedance. The equivalent resistance is equal to R, and

the equivalent capacitance is equal to C_H.

This architecture improves the circuit performance; however, there are still a few concerns that need to be addressed. First, when SW_1 and SW_2 are both opened, there is no feedback path for the output amplifier; the amplifier is operating open loop. Second, the hold capacitor at the inverting input of the amplifier can cause additional phase shift, reducing the op amp's phase margin (PM).

Pole-Zero Architecture for the Deglitch Circuit

With a slight change in the amplifier feedback network, the circuit can address the phase-shift problem. As shown in **Figure 5**, the equivalent impedance at both sides of switches SW1 and SW2 are matched. This circuit effectively adds a zero at the pole location in the amplifier feedback network that compensates for the added phase shift and reduced phase margin of Figure 4.

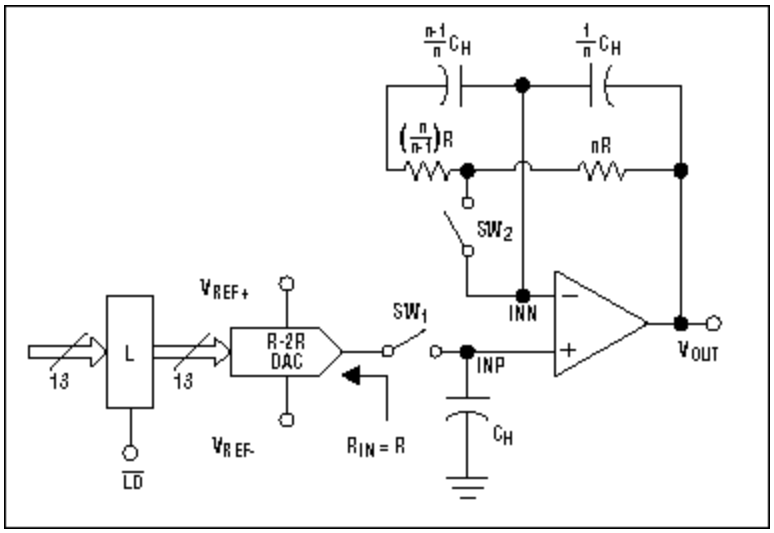

Figure 5. Complete architecture.

With this configuration, there is no phase shift from V_{OUT} to V_{INN-}. When SW_2 opens, C_1 and C_2 maintain the negative feedback. For the pole-zero cancellation, the equivalent feedback network is shown in **Figure 6**.

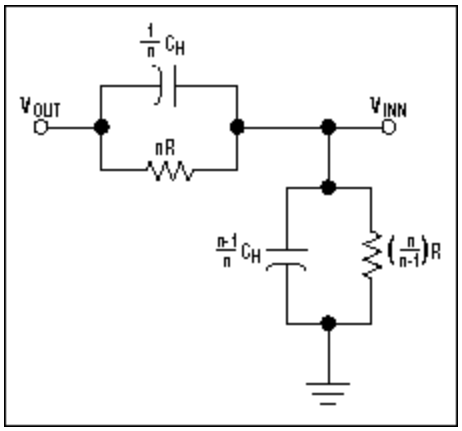

Figure 6. Equivalent circuit of feedback network.

Mathematically, the advantage of this circuit, namely the pole-zero cancellation, is derived as follows:

$$C_1 + C_2 = \left(\frac{n-1}{n}\right) \bullet C_H + \left(\frac{1}{n}\right) \bullet C_H = C_H$$

$$R_1 // R_2 = \left[\left(\frac{n}{n-1}\right) \bullet R\right] // (nR) = R$$

$$\frac{1}{Z_1} = \left(\frac{n-1}{n}\right) \bullet \frac{1}{R} + \left(\frac{n-1}{n}\right) \bullet SC$$

$$\frac{1}{Z_2} = \left(\frac{1}{n}\right) \bullet \frac{1}{R} + \left(\frac{1}{n}\right) \bullet SC$$

$$\frac{V_{INN}}{V_{OUT}} = \frac{Z_1}{Z_1 + Z_2} = \frac{1/Z_1}{1/Z_1 + 1/Z_2}$$

$$\frac{V_{INN}}{V_{OUT}} = \frac{\left(\frac{1}{n}\right) \bullet \frac{1}{R} + \left(\frac{1}{n}\right) \bullet SC}{\left[\left(\frac{n-1}{n}\right) \bullet \frac{1}{R} + \left(\frac{n-1}{n}\right) \bullet SC\right] + \left[\left(\frac{1}{n}\right) \bullet \frac{1}{R} + \left(\frac{1}{n}\right) \bullet SC\right]}$$

$$\frac{V_{INN}}{V_{OUT}} = \frac{\left(\frac{1}{n}\right) \bullet \left[\frac{1}{R} + SC\right]}{\left[\left(\frac{1}{n}\right) \bullet \frac{1}{R} + \left(\frac{n-1}{n}\right) \bullet \frac{1}{R}\right] + \left[\left(\frac{1}{n}\right) \bullet SC + \left(\frac{n-1}{n}\right) \bullet SC\right]}$$

$$\frac{V_{INN}}{V_{OUT}} = \left(\frac{1}{n}\right) \bullet \frac{[1/R + SC]}{[1/R + SC]} = \frac{1}{n}$$

Test Results

This smart deglitch circuit for the voltage DAC technique is currently used in the MAX5839, a 13-bit, octal, high-voltage DAC. Test measurements reveal that the digital-to-analog glitch energy is up to 10 times' smaller than that of other devices on the market. The following plot shows the test results.

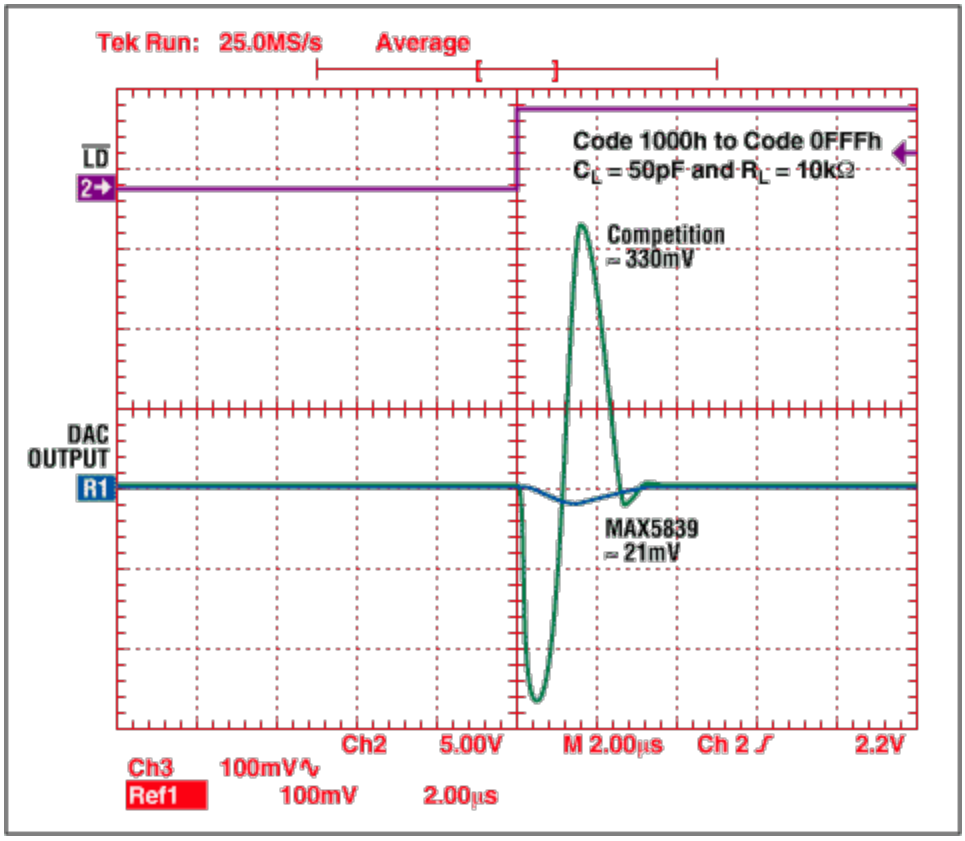

Figure 7. Glitch amplitude during a major-carry transition.

Conclusions

Using a T/H amplifier technique for deglitch circuits, we achieve very small glitches (typically 10mV to 20mV) at the DAC output during major-carry transitions. By implementing pole-zero cancellation in the RC feedback network, the additional phase shift due to the hold capacitor is eliminated and the stability of the output amplifier is maintained. When the sampling switch is opened, negative feedback is still employed via capacitors C_1 and C_2. Additionally, base-current cancellation eliminates the voltage offset due to $R_{SW} \times I_{base}$. Finally, by properly choosing the gain "n" of the output amplifier, we can use process constraints (which could otherwise complicate the design) to our advantage.

Related Parts	
MAX5839	Octal, 13-Bit Voltage-Output DAC with Parallel Interface

More Information
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