

# FDW6923

# P-Channel 2.5V Specified PowerTrench® MOSFET with Schottky Diode

### **General Description**

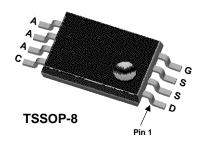
This P-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It is combined with a low forward drop Schottky diode which is isolated from the MOSFET, providing a compact power solution for asynchronous DC/DC converter applications.

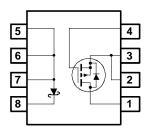
### **Applications**

• DC/DC conversion

### **Features**

- -3.5 A, -20 V.  $R_{DS(ON)}$  = 0.045  $\Omega$  @  $V_{GS}$  = -4.5 V  $R_{DS(ON)}$  = 0.075  $\Omega$  @  $V_{GS}$  = -2.5 V
- V<sub>F</sub> < 0.55 V @ 1 A
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS}(\mbox{\scriptsize ON})}$
- Low profile TSSOP-8 package





### MOSFET Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	-20	V
V <sub>GSS</sub>	Gate-Source Voltage	± 12	V
I <sub>D</sub>	Drain Current - Continuous (Note 1)	<del>-</del> 3.5	Α
	- Pulsed	-30	
P <sub>D</sub>	MOSFET Power Dissipation (minimum pad) (Note 1) Schottky Power Dissipation (minimum pad) (Note 1)	1.2 1.0	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

**Schottky Maximum Ratings** 

V <sub>RRM</sub>	Repetitive Peak Reverse Voltage	20	V
I <sub>F</sub>	Average Forward Current	1.5	Α
I <sub>FM</sub>	Peak Forward Current	30	Α

### **Thermal Characteristics**

$R_{\theta JA}$	R <sub>BJA</sub> Thermal Resistance, Junction-to-Ambient		MOSFET: 115	°C/W
	(minimum pad)	(Note 1)	Schottky: 130	

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
6923	FDW6923	13"	16mm	2500 units

Symbol	Parameter	Test Condition	ons Min	Тур	Max	Units
Off Char	acteristics		•	•	•	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-20			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Reference	ed to25°C	-16		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V},  V_{GS} = 0$	V		-1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	$V_{GS} = -12 \text{ V},  V_{DS} = 0$	) V		-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = 12 \text{ V}, \qquad V_{DS} = 0$	V		100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	<b>√</b> −0.6	-1.0	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$ , Reference	ed to25°C	3		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$\begin{array}{c} V_{GS} = -4.5 \text{ V},  I_D = -3.5 \\ V_{GS} = -2.5 \text{ V},  I_D = -2.5 \\ V_{GS} = -4.5 \text{ V},  I_D = -3.5 \\ V_{GS} = -4.5 \text{ V},  V_{DS} = -4.5 \text{ V}, \end{array}$	2.7 A	36 56 49	45 75 72	mΩ
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5 \text{ V}, \qquad V_{DS} =$	−5 V −15			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_D = -5 \text{ V}$	3.5A	13.2		S
Dvnamio	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -10 \text{ V},  V_{GS} =$	0 V.	1030		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz	,	280		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			120		pF
Switchin	ng Characteristics (Note 2)		•	•	•	
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -5 \text{ V}.$ $I_D = -$	1 A.	11	20	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = -5 \text{ V}, \qquad I_{D} = -6 \text{ V}$	= 6 Ω	18	32	ns
$t_{d(off)}$	Turn-Off Delay Time			34	55	ns
t <sub>f</sub>	Turn-Off Fall Time			34	55	ns
$\overline{Q_g}$	Total Gate Charge	$V_{DS} = -5V$ , $I_{D} = -3$	3.5 A,	9.7	16	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -4.5 V	,	2.2		nC
$Q_{gd}$	Gate-Drain Charge			2.4		nC
Drain-S	ource Diode Characteristics	and Maximum Ratir	nas			
Is	Maximum Continuous Drain-Source				-1.25	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_{S} = -1.25$	A (Note 2)	-0.6	-1.2	V
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = 12 \text{ V}, \qquad V_{DS} = 0$	V		100	nA
Schottky	/ Diode Characteristics		<u>.</u>			
I <sub>R</sub>	Reverse Leakage	V <sub>R</sub> = 20V	T <sub>J</sub> =25°C	0.6	50	μA
		_	T <sub>J</sub> =125°C	1	8	mA
V <sub>F</sub>	Forward Voltage		T <sub>J</sub> =25°C	0.48	0.55	V
'		'   <del> </del>	T <sub>J</sub> =125°C	0.42	0.50	V
Ст	Junction Capacitance	V <sub>R</sub> = 10V		50		pF

#### Notes

<sup>1.</sup>  $R_{\theta,JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta,JC}$  is guaranteed by design while  $R_{\theta,CA}$  is determined by the user's board design.

 $<sup>\</sup>rm R_{\rm \theta JA}$  is 115 °C/W for the MOSFET and 130°C/W for the Schottky Diode when mounted on a minimum pad.

**<sup>2.</sup>** Pulse Test: Pulse Width <  $300\mu$ s, Duty Cycle < 2.0%

# **Typical Characteristics**

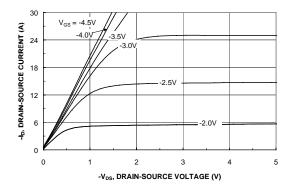


Figure 1. On-Region Characteristics.

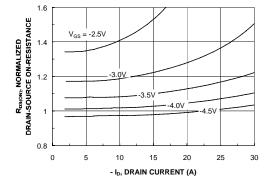


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

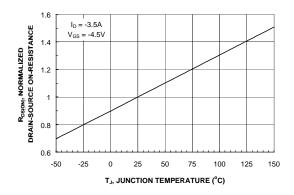


Figure 3. On-Resistance Variation with Temperature.

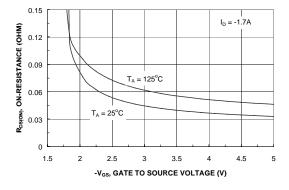


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

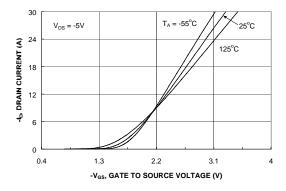


Figure 5. Transfer Characteristics.

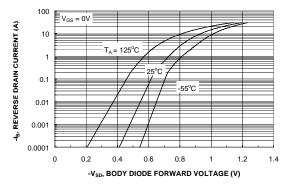
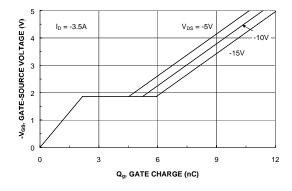


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



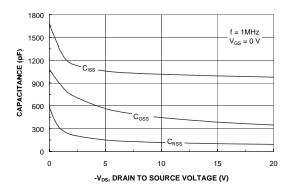


Figure 7. Gate Charge Characteristics.

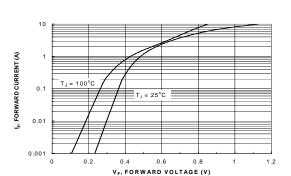


Figure 8. Capacitance Characteristics.

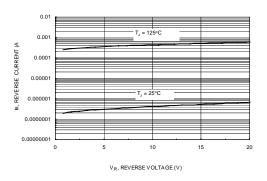


Figure 9. Schottky Diode Forward Voltage.



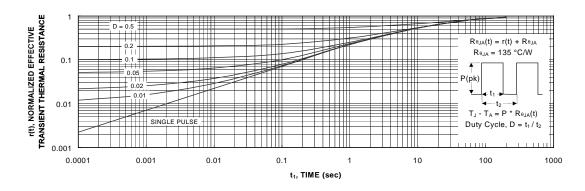


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1. Transient thermal response will change depending on the circuit board design.





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