Click here for production status of specific part numbers.

MAX38904A/B/C/D

1.7V–5.5V_{IN}, 2A Low Noise LDO Linear Regulators in TDFN and WLP

General Description

The MAX38904 is a 1.7V–5.5V V_{IN}, low-noise linear regulator that delivers up to 2A of output current with only 5.1µV_{RMS} of output noise from 10Hz to 100kHz. The regulator maintains ±1% output accuracy over a wide input voltage range, requiring only 100mV of input-to-output headroom at full load. The 1.3mA no-load supply current is independent of dropout voltage.

The output voltage on MAX38904B can be adjusted to a value in the range of 0.6V to 5.0V by using two external resistors. The MAX38904B also includes an active-high POK signal for trouble-free load startup.

The MAX38904A has nine pin-selectable output voltages 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.1V, 3.3V, 4.0V, and 5V.

The wafer-level package (WLP) versions of the MAX38904 are available as C and D variants. The MAX38904C uses external feedback resistors for adjusting the output voltage, while the MAX38904D has factory preset output voltages over the range of 0.7V to 5.0V in 50mV steps.

All versions include a programmable output soft-start rate, output overcurrent, and thermal overload protection.

The MAX38904A/B are offered in a 3mm x 3mm, 14-pin TDFN package, while the MAX38904C/D are available in 5 x 3 bump, 2.2mm x 1.37mm WLP, 0.4mm pitch.

Applications

- Communication Systems, Test Equipment, Medical Equipment
- High-End Audio Systems
- High-Resolution Data Acquisition Systems

Benefits and Features

- Delivers Flexible Operating Range
  - 1.7V to 5.5V Input Voltage Range
  - 0.6V to 5.0V Programmable Output Voltage
  - 2A Maximum Output Current
  - 100mV Maximum Dropout at 2A Load
  - < 1.5µA Shutdown Supply Current
- Reduces Noise and Improves Accuracy
  - ±1% DC Accuracy Over Load, Line, and Temperature
  - 5.1µV_{RMS} Output Noise, 10Hz to 100kHz
  - 1.3mA Quiescent Supply Current
  - > 70dB PSRR at 10kHz
- Enables Ease-of-Use and Robust Protection
  - Stable with 8µF (Min) Output Capacitance
  - Programmable Soft-Start Rate
  - Overcurrent and Overtemperature Protection
  - Output-to-Input Reverse Current Protection
  - Power-OK Status Pin
- Reduces Size, Improves Reliability
  - 3mm x 3mm 14-pin TDFN Package and 2.2mm x 1.37mm, 5 x 3 Bump, 0.4mm Pitch WLP
  - -40ºC to 125ºC Operating Temperature

***Ordering Information* appears at end of data sheet.**

19-100443; Rev 2; 3/19

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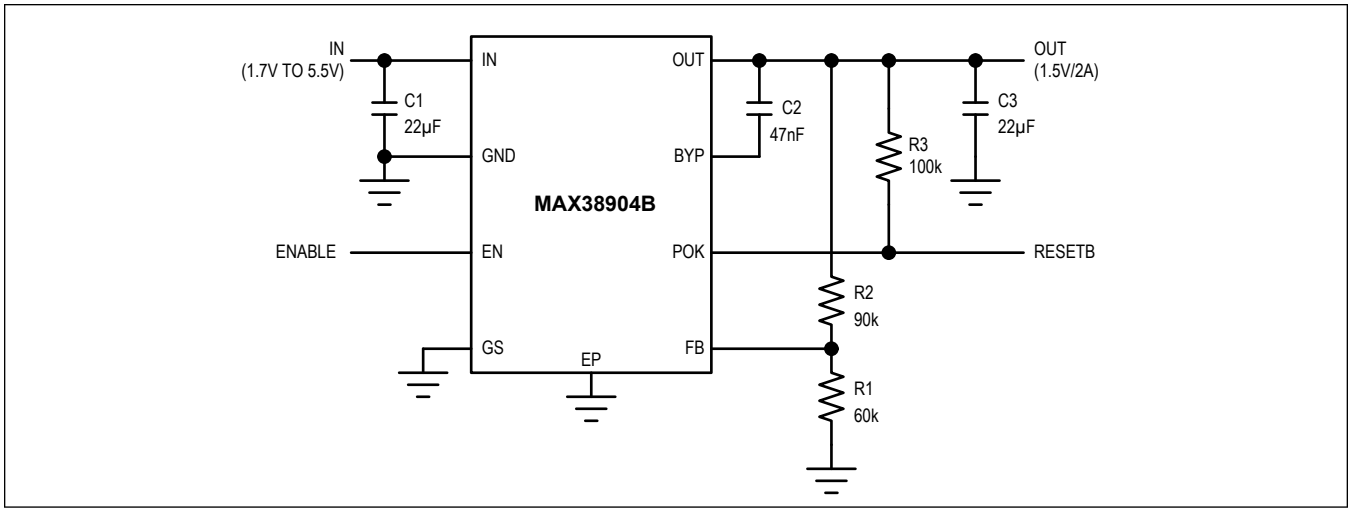
Simplified Block Diagram



Absolute Maximum Ratings

IN, OUT, SELA, SELB, EN, POK, OUTS, FB, GS to GND ..-0.3V to +6V
BYP ..... -0.3V to +2V
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation TDFN (T_A = +70°C, derate 24.4mW/°C above +70°C.) 1951mW
Continuous Power Dissipation WLP (T_A = +70°C, derate 16.4mW/°C above +70°C.) 1312mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	T1433+2C
Outline Number	21-0137
Land Pattern Number	90-0063
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W

WLP

Package Code	N151B2+1
Outline Number	21-100315
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	61.55°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 3.6V, T_J = -40°C to +125°C, C_{BYP} = 47nF, C_{IN} = 22µF, C_{OUT} = 22µF, *Typical Operating Circuit*, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by Output Accuracy		1.7		5.5	V
Input Undervoltage Lockout	V_{UVLO}	V_{IN} rising, 100mV hysteresis		1.5	1.6	1.7	V
Output Voltage Range	V_{OUT}	V_{IN} > V_{OUT} + 0.1V		0.6		5.0	V
Output Capacitance	C_{OUT}	For stability and proper operation		8	22		µF
Supply Current	I_{IN}	V_{EN} = V_{IN} = 3.6V, I_{OUT} = 0mA			1300		µA
		V_{EN} = 0V	T_A = +25°C		0.04	1.5	
			T_A = 125°C		1.5		
FB Regulation Accuracy (MAX38904B/C Only)	ACC	I_{OUT} from 0.1mA to 2A, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V		0.594	0.6	0.606	V
OUT Regulation Accuracy (MAX38904A/D Only)	ACC	I_{OUT} from 0.1mA to 2A, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V		-1		+1	%
Load Regulation		V_{IN} = 2.8V, V_{OUT} = 2.5V, I_{OUT} from 0.1mA to 2A			0.032		%
Load Transient		Output Voltage deviation with a load change of I_{OUT} = 50mA to 2.0A to 50mA, with t_{RISE} = t_{FALL} = 1µs			50		mV_{P-P}
Line Regulation		V_{IN} from 2.8V to 5.5V, V_{OUT} = 2.5V, I_{OUT} = 800mA			0.054		%/V
Line Transient		V_{IN} = 4V to 5V to 4V, I_{OUT} = 2A, t_{RISE} = t_{FALL} = 5µs			3		mV_{P-P}
Dropout Voltage (Note 2)		I_{OUT} = 2A	V_{IN} = 3.6V		47	100	mV
			V_{IN} = 2.5V (Note 3)		65	200	
			V_{IN} = 1.7V		100	300	
Current Limit		V_{OUT} = 95% of regulation, V_{IN} - V_{OUT} = 0.5V, V_{IN} = 3.6V		2.2	2.8	3.4	A
Output Noise		I_{OUT} = 100mA, C_{BYP} = 100nF	f = 10Hz to 100kHz		5.1		$µV_{RMS}$
Power Supply Rejection Ratio	PSRR	V_{IN} = V_{OUT} + 400mV, I_{OUT} = 1.6A	f = 1kHz		70		dB
			f = 10kHz		70		
			f = 100kHz		60		
			f = 1MHz		40		
BYP Capacitor Range	C_{BYP}	Regulator Remain Stable		0.001		0.1	µF
BYP Soft-Start Current		From BYP to GND during startup			50		µA
EN Input Threshold		V_{IN} from 1.7V to 5.5V	EN rising		0.8	1.2	V
EN Input Threshold		V_{IN} from 1.7V to 5.5V	EN falling	0.4	0.7		V

Electrical Characteristics (continued)

(V_{IN} = 3.6V, T_J = -40°C to +125°C, C_{BYP} = 47nF, C_{IN} = 22µF, C_{OUT} = 22µF, *Typical Operating Circuit*, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EN Input Leakage Current		V_{EN} from 1.7V to 5.5V	T_A = +25ºC	-1	+0.001	+1	µA
		V_{EN} from 1.7V to 5.5V	T_A = +125°C		0.01		
POK Threshold (MAX38904B Only)		V_{OUT} when POK switches	V_{OUT} rising	88	91	94	%
			V_{OUT} falling		88		
POK Voltage, Low (MAX38904B Only)	V_{OL}	I_{POK} = 1mA			10	100	mV
POK Leakage Current (MAX38904B Only)		V_{POK} = 5.5V	T_A = +25°C	-0.1	+0.001	+0.1	µA
			T_A = +125°C		0.01		
SELA/B Input Resistance (MAX38904A Only)	$R_{INSELA/B}$	When shorted to GND or IN				500	Ω
		When Hi-Z		1			MΩ
SELA/B Input Capacitance (MAX38904A Only)	$C_{INSELA/B}$	When Hi-Z				10	pF
IN Reverse-Current Threshold	I_{IN_REV}	V_{OUT} = 3.6V, when V_{IN} falls to 0V			800		mA
Thermal Shutdown Threshold		T_J when output turns on/off	T_J rising		165		ºC
			T_J falling		150		

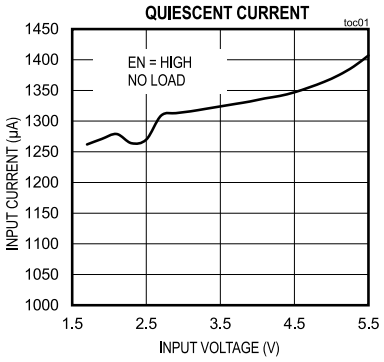
Note 1: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.

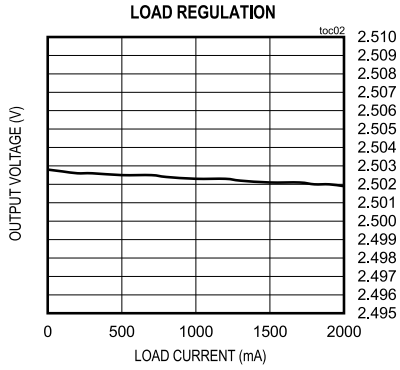
Note 2: Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 95% of its nominal value.

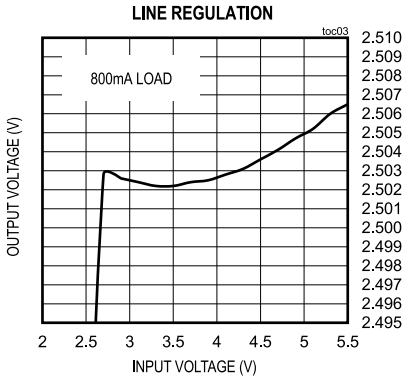
Note 3: Guaranteed by design and characterization.

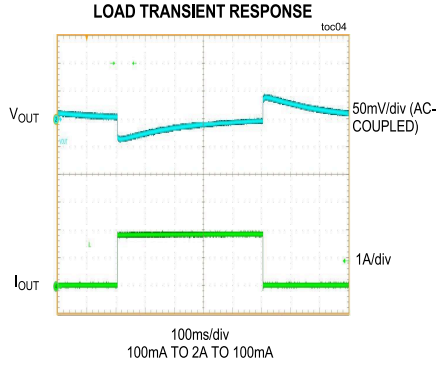
Typical Operating Characteristics

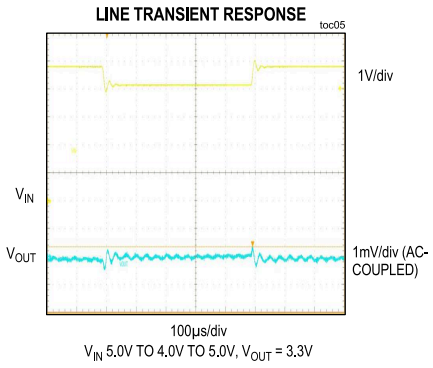
(MAX38904BATD+, V_{IN} = 3.6V, V_{OUT} = 2.5V, C_{BYP} = 47nF, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25ºC, unless otherwise noted)

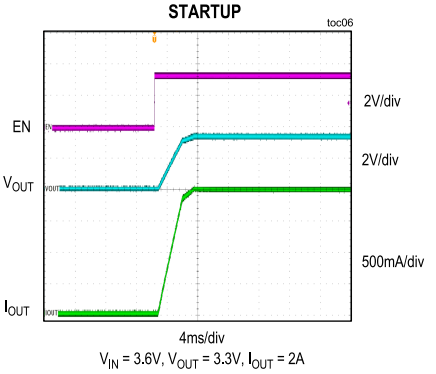


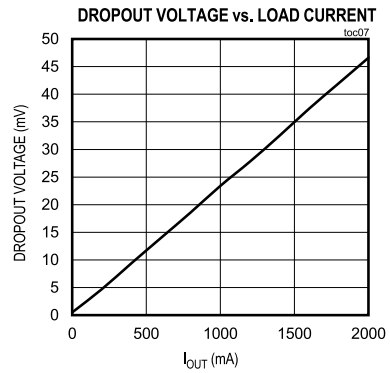


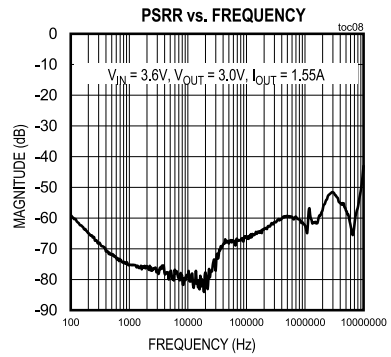


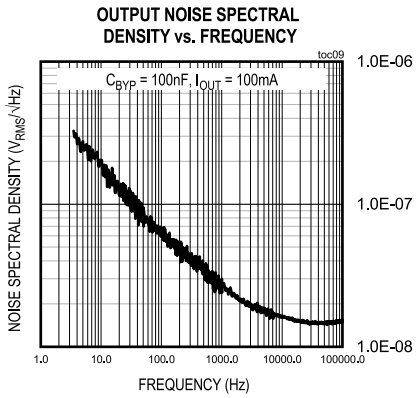






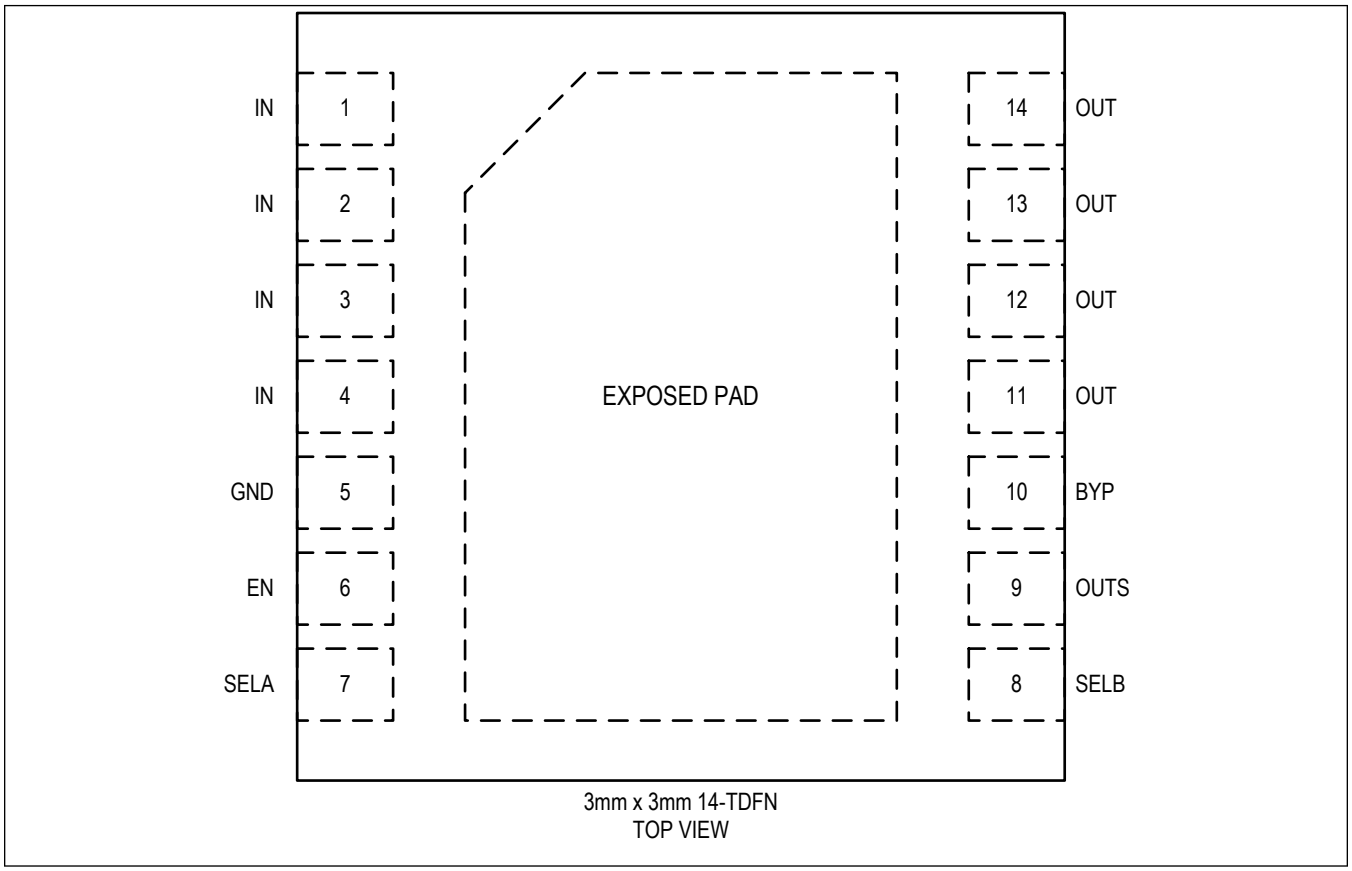






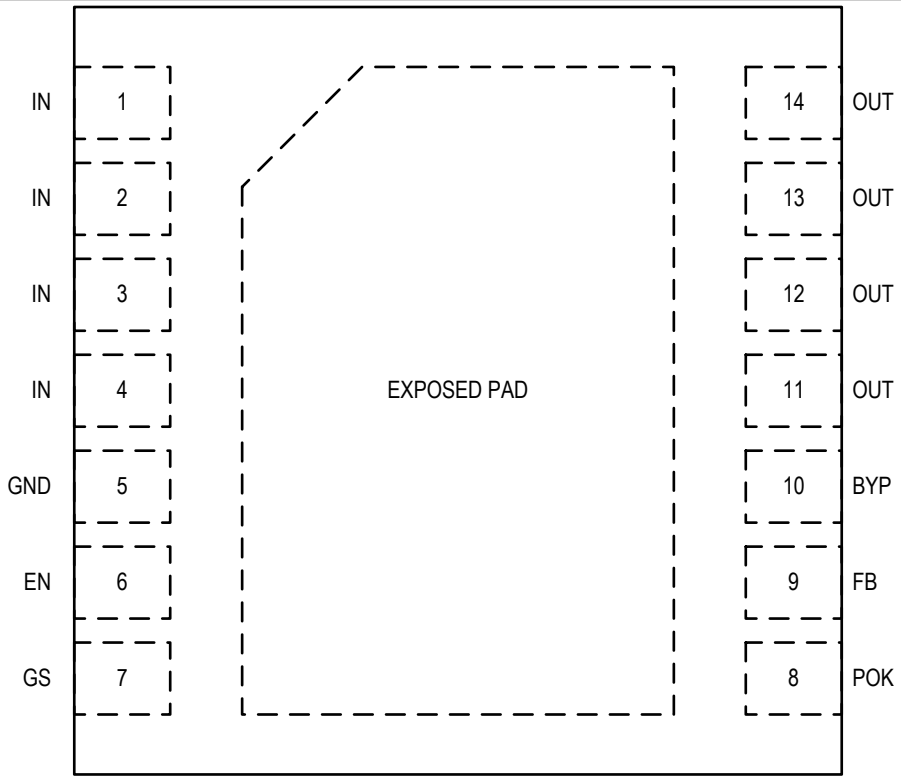
Pin Configurations

MAX38904A



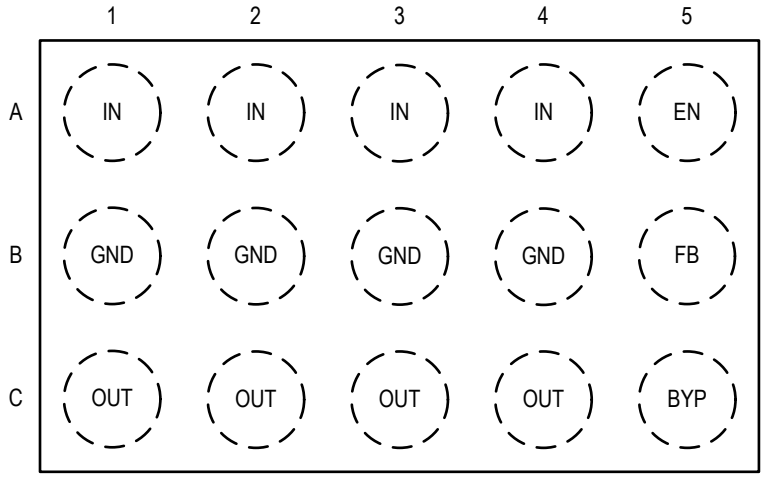
3mm x 3mm 14-TDFN
TOP VIEW

MAX38904B



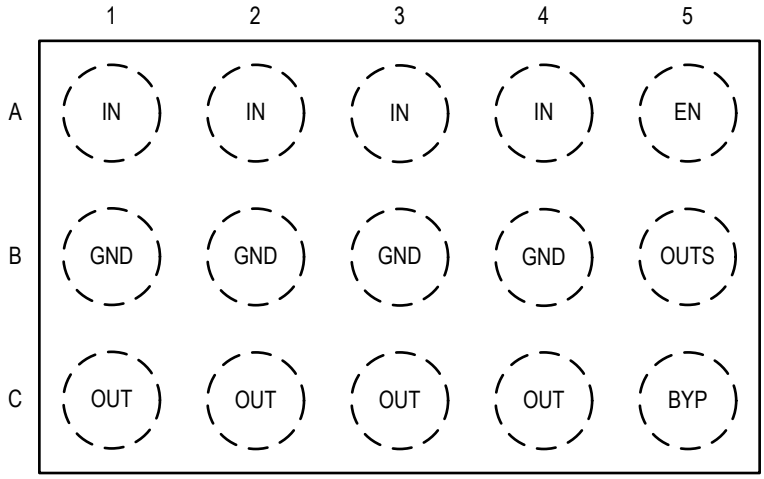
3mm x 3mm 14-TDFN
TOP VIEW

MAX38904C



3 x 5 BUMP 0.4mm PITCH WLP
TOP VIEW

MAX38904D



3 x 5 BUMP 0.4mm PITCH WLP
TOP VIEW

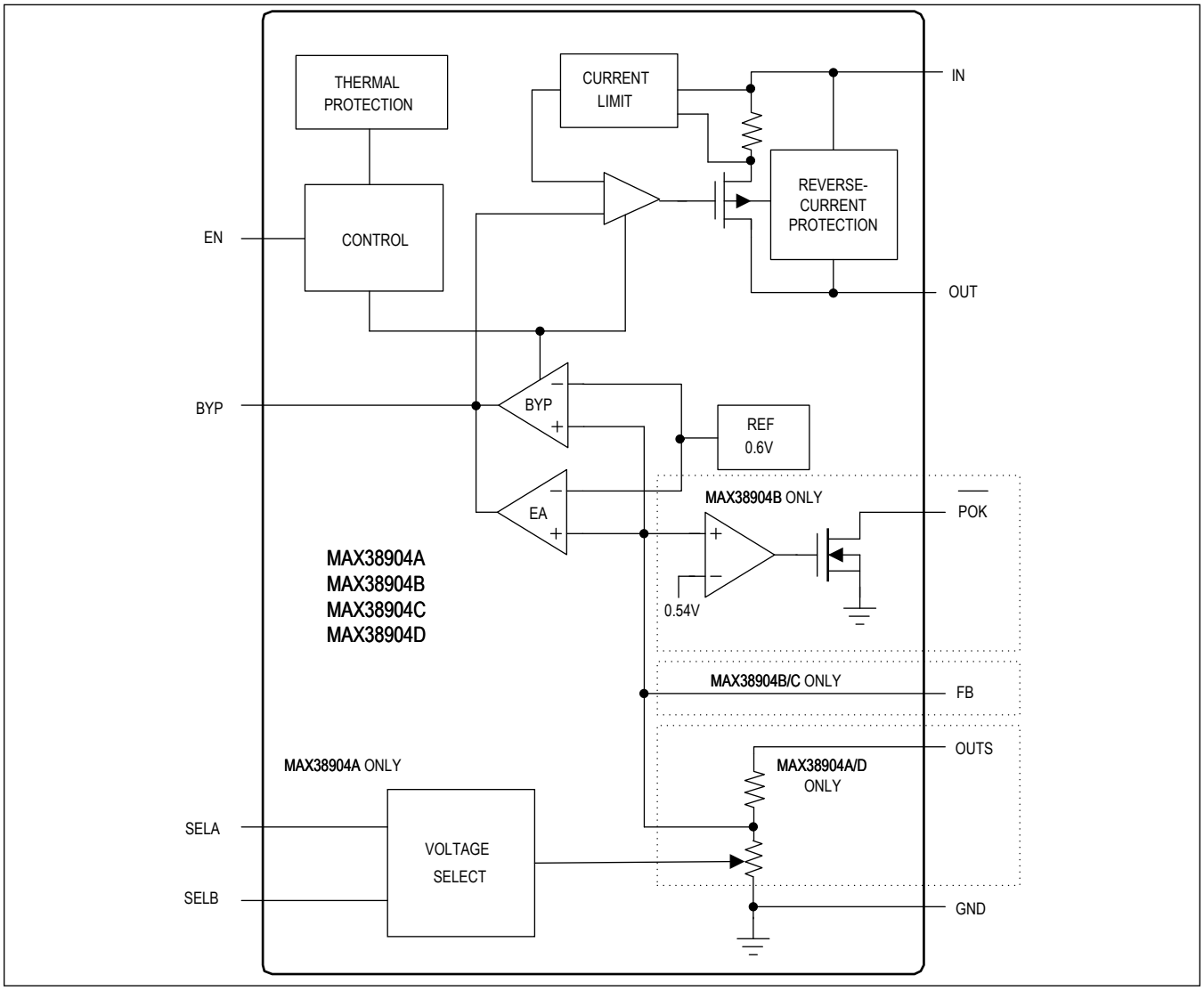
Pin Description

PIN				NAME	FUNCTION
MAX38904A	MAX38904B	MAX38904C	MAX38904D		
1, 2, 3, 4	1, 2, 3, 4	A1, A2, A3, A4	A1, A2, A3, A4	IN	Regulator Supply Input. Connect to a voltage between 1.7V and 5.5V and bypass with a 22µF capacitor from IN to GND.
5	5	B1, B2, B3, B4	B1, B2, B3, B4	GND	Regulator Ground. Bring IN and OUT bypass capacitor GND connections to this pin for best performance.
6	6	A5	A5	EN	Enable Input. Connect this pin to a logic signal to enable (V_{EN} high) or disable (V_{EN} low) the regulator output. Connect to IN to keep the output enable whenever a valid supply voltage is present.
7	—	—	—	SELA	Output Select Input. Connect to GND, IN, or Hi-Z to select one of three states. The state of the SELA and SELB pins are read when the device is enabled and used to select one of nine output voltages.
—	7	—	—	GS	Ground Sense. Connect GS to GND.
8	—	—	—	SELB	Output Select Input. Connect to GND, IN, or Hi-Z to select one of three states. The state of the SELA and SELB pins are read when the device is enabled and used to select one of nine output voltages.
—	8	—	—	POK	Active-High Power-OK Output. Connect a pullup resistor from this pin to a supply to create a reset signal that goes high after the regulator output has reached its regulation voltage.
9	—	—	B5	OUTS	Output Voltage Sense Input. Connect to the load at a point where accurate regulation is required to eliminate resistive metal drops.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX38904A	MAX38904B	MAX38904C	MAX38904D		
—	9	B5	—	FB	Feedback Divider Input. Connect a resistor divider string from OUT to GND with the midpoint tied to this pin to set the output voltage. In the *Typical Application Circuits*, V_{OUT} = 0.6V x (1 + R2/R1).
10	10	C5	C5	BYP	Bypass Capacitor Input. Connect a 0.001µF to 0.1µF capacitor between OUT and BYP to reduce output noise and set the regulator soft-start rate.
11, 12, 13, 14	11, 12, 13, 14	C1, C2, C3, C4	C1, C2, C3, C4	OUT	Regulator Output. Sources up to 2A at the output regulation voltage. Bypass with a 22µF (8µF minimum, including voltage derating) low ESR (< 0.03Ω) capacitor to GND.
EP	EP	—	—	EP	Exposed Pad (TDFN Only). Connect the exposed pad to a ground plane with low thermal resistance to ambient to provide best heat sinking.

Simplified Functional Diagram



Detailed Description

The MAX38904 is a high-performance PMOS linear regulator that is optimized for low noise, high input supply rejection, low dropout voltage, and small solution size. It can deliver up to a maximum load current of 2A while maintaining a low dropout voltage of 47mV. An enable input allows the regulator to be powered up and down, while an internal soft-start circuit controls the in-rush current at the input. SELA and SELB inputs are provided on A version for selecting one of nine output voltages and a power-OK output is provided on the B version for system power-up sequencing.

Enable (EN)

The MAX38904 includes an enable pin (EN). Pull EN low to shut down the output, or drive EN high to enable the output. If a separate shutdown signal is not available, connect EN to IN.

Bypass (BYP)

The capacitor connected from BYP to OUT filters noise at the reference, feedback resistors and regulator input stage. It provides a high speed feedback path for improved transient response. A 10nF capacitor rolls off noise at around 32Hz.

The slew rate of the output voltage during startup is also determined by the BYP capacitor. A 10nF capacitor sets the slew rate to 5V/ms. This startup rate results in a 110mA slew current drawn from the input at startup to charge 22µF output capacitance.

The BYP capacitor value can be adjusted from 1nF to 100nF to change the startup slew rate according to the following formula:

$$\text{Startup Slew Rate} = \frac{5V}{\text{ms}} \times \frac{10\text{nF}}{C_{BYP}}$$

where C_{BYP} is in nF.

Note that this slew rate applies only at startup. Recovery from a short-circuit will occur at a slew rate approximately 500 times slower.

Also, note that being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Protection Features

The MAX38904 is fully protected from an output short-circuit by a current limiting and thermal overload circuit. If the output is shorted to GND, the output current is limited to 2.8A (typ). Under these conditions, the device quickly heats up. When the junction temperature reaches 165°C, a thermal limit circuit shuts the output device off. Once the device cools to 150°C, the output turns back on in an attempt to reestablish regulation. If the fault persists, the output current cycles on and off as the junction temperature slews between 150°C and 165°C.

The MAX38904 is also protected against reverse current when the output voltage is higher than the input. In the event that extra output capacitance is used at the output, a power down transient at the input would normally cause a large reverse-current through a conventional regulator. The MAX38904 includes a reverse-voltage detector that trips when IN drops 10mV below OUT shutting off the regulator and opening the PMOS body diode connection preventing any reverse current.

Output Voltage Configuration (MAX38904A)

The MAX38904A has two configuration pins, SELA and SELB, that are read during power-up to determine the output regulation voltage.

Table 1. MAX38904A Output Configuration Table

V_{OUT} (V)	SELA	SELB
1.2	Hi-Z	IN
1.5	IN	Hi-Z
1.8	Hi-Z	GND
2.5	Hi-Z	Hi-Z
3.0	GND	GND
3.1	GND	IN
3.3	GND	Hi-Z
4.0	IN	GND
5.0	IN	IN

Output Voltage Configuration (MAX38904B/C)

The MAX38904B and MAX38904C use external feedback resistors to set the output regulation voltage as shown in the Typical Operating Circuit. The output voltage can be set form 0.6V to 5.0V. Set the lower feedback resistor R1 to 300kΩ or less to minimize FB input bias current error. Then, calculate the value of the upper feedback resistor R2 as follows:

$$R2 = R1 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} is the feedback regulation voltage of 0.6V.

To set the output to 2.4V, for example, R2 should be:

$$R2 = 300k\Omega \times \left(\frac{2.4V}{0.6V} - 1\right) = 900k\Omega$$

Output Voltage Configuration (MAX38904D)

The MAX38904D output voltage comes preprogrammed to values listed below. Additionally, any output voltage between 0.7V and 5.0V in 50mV steps can be factory programmed and special ordered. Contact a Maxim Integrated representative to order preprogrammed parts.

Table 2. MAX38904D Output Configuration Table

PART NUMBER	V_{OUT} (V)
MAX38904DANL12	1.2
MAX38904DANL15	1.5
MAX38904DANL18	1.8
MAX38904DANL20	2.0
MAX38904DANL25	2.5
MAX38904DANL27	2.7
MAX38904DANL30	3.0
MAX38904DANL33	3.3
MAX38904DANL36	3.6
MAX38904DANL50	5.0
MAX38904DANL__	*

** For other preprogrammed voltage selections, contact a Maxim Integrated representative.*

Power-OK (MAX38904B)

The MAX38904B includes an additional open-drain output, POK, that goes high to indicate the output voltage is in regulation. Connect a pullup resistor from this pin to an external supply. During startup, POK stays low until the output voltage rises to 91% (typ) of its regulation level. If an overload event occurs at the output, or the output is shutdown, POK goes low.

Input Capacitor

A 22µF ceramic capacitor is recommended for the input. Select a capacitor that does not degrade significantly over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

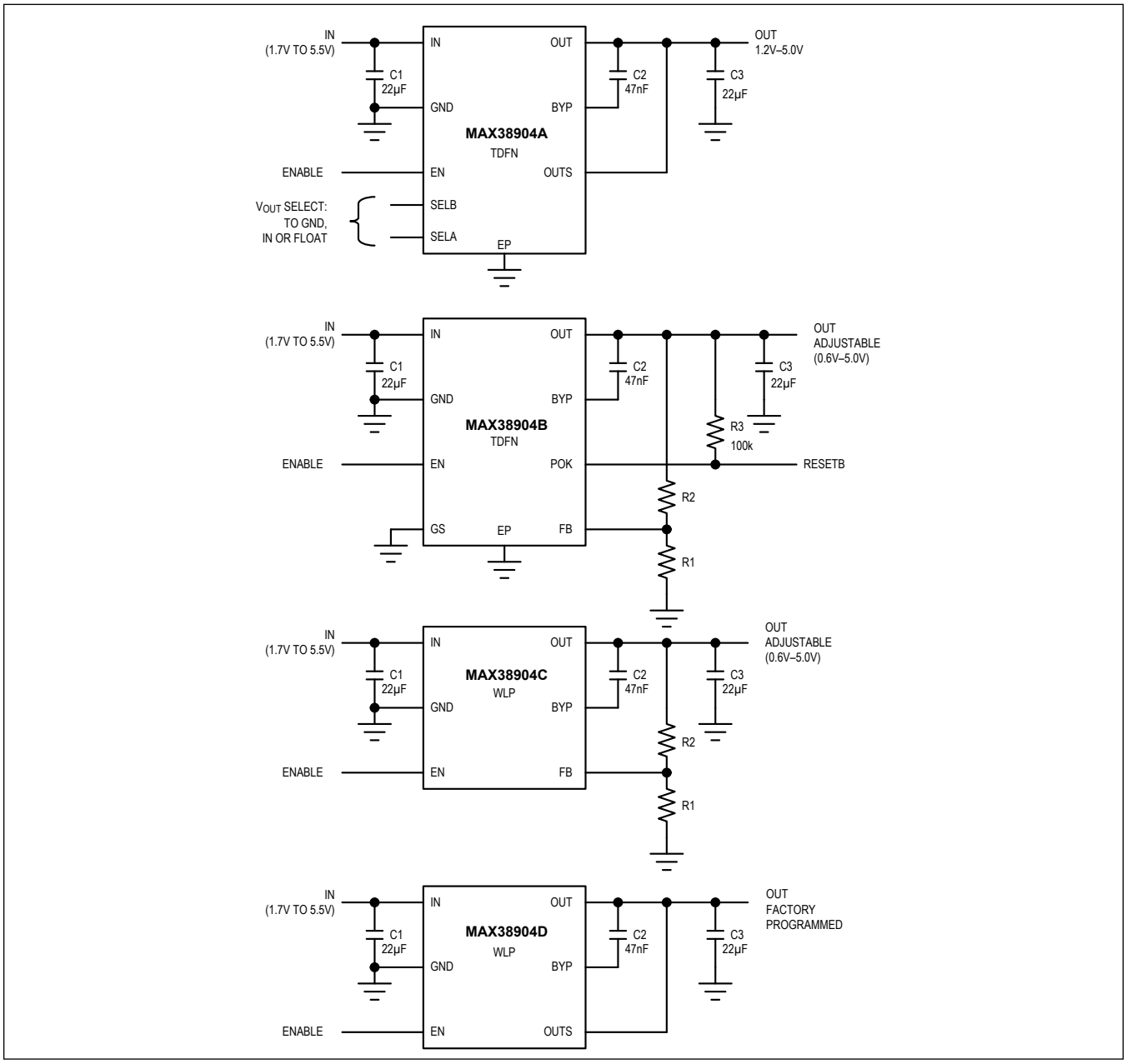
Output Capacitor

A minimum of 8µF capacitance is required at OUT to ensure stable operation. Select a ceramic capacitor that maintains its capacitance (8µF minimum) over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

Thermal Considerations

The MAX38904 is packaged in a 14-pin 3mm x 3mm TDFN package with an exposed paddle. The exposed paddle is the main thermal path for heat to escape the IC, and therefore, must be connected to a ground plane with thermal vias to allow heat to dissipate from the device. Thermal properties of the package are given in the *Package Information* section.

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FEATURES
MAX38904AATD+	-40°C to +125°C	14-pin, 3mm x 3mm, TDFN	Pin-Selectable Output Voltage, Enable
MAX38904BATD+	-40°C to +125°C	14-pin, 3mm x 3mm, TDFN	External Resistor Feedback, POK Output with Delay, Enable
MAX38904CANL+*	-40°C to +125°C	15-pin, 5 x 3, 0.4mm pitch, WLP	External Resistor Feedback, Enable
MAX38904DANL__+*	-40°C to +125°C	15-pin, 5 x 3, 0.4mm pitch, WLP	Preprogrammed Output Voltage, Enable
MAX38904DANL15+*	-40°C to +125°C	15-pin, 5 x 3, 0.4mm pitch, WLP	Factory Programmed to 1.5V, Enable

#Denotes a RoHS-compliant device that may include lead(Pb) that is exempt under the RoHS requirements.

T = Tape-and-reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/18	Initial release	—
1	12/18	Updated title of data sheet and *Ordering Information*	1–16
2	3/19	Updated Table 2 and *Ordering Information*	14, 16