

Interfacing the **ADL5372** I/Q Modulator to the **AD9779A** Dual-Channel, 1 GSPS High Speed DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides a simple, elegant interface between the **ADL5372** I/Q modulator and the **AD9779A** high speed digital-to-analog converter (DAC). The **ADL5372** and the **AD9779A** are well-matched devices because they have the same bias levels and similarly high signal-to-noise ratios (SNR). The matched bias levels of 500 mV allow for a glueless interface; there is no need for a level shifting network, which can add noise and insertion loss along with extra components. The addition of the swing limiting resistors (RSLI and RSLQ) allows the DAC swing to scale appropriately without loss of resolution or of the 0.5 V bias level. The high SNR of each device preserves a high SNR through the circuit.

CIRCUIT DESCRIPTION

The **ADL5372** interfaces with minimal components to members of Analog Devices, Inc., family of TxDAC® converters. The baseband inputs of the **ADL5372** require a dc common-mode bias voltage of 500 mV. With each **AD9779A** output swinging from 0 mA to 20 mA, adding a single 50 Ω resistor to ground from each of the DAC outputs provides the desired 500 mV dc bias. For example, with four 50 Ω resistors in place, the voltage swing on each pin is 1 V p-p, which results in a differential voltage swing of 2 V p-p on each input pair.

By adding the RSLI and RSLQ resistors to the interface, the output swing of the DAC reduces without any loss of DAC resolution. Place each resistor as a shunt between each side of the differential pair, as shown in Figure 1. It has the effect of reducing the ac swing without changing the dc bias already established by the 50 Ω resistors and the DAC output current.

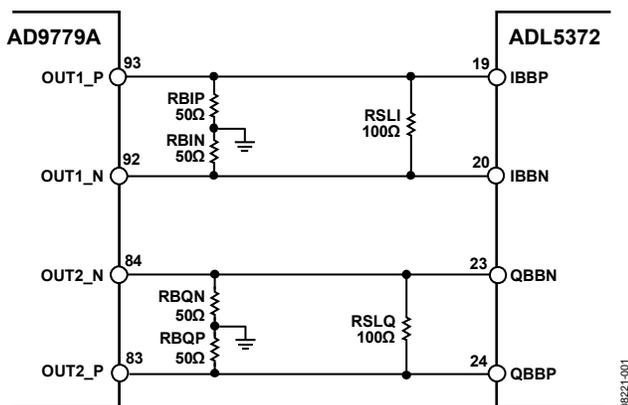


Figure 1. Interface Between the **AD9779A** and **ADL5372** with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the **ADL5372** Baseband Inputs (Simplified Schematic)

Choose the value of this ac swing limiting resistor based on the desired ac voltage swing. Figure 2 shows the relationship between the swing limiting resistor and the peak-to-peak ac swing that it produces when using 50 Ω bias setting resistors. Note that all Analog Devices I/Q modulators present a relatively high input impedance on their baseband inputs (typically >1 kΩ). As a result, the input impedance of the I/Q modulator has no effect on the scaling of the DAC output signal.

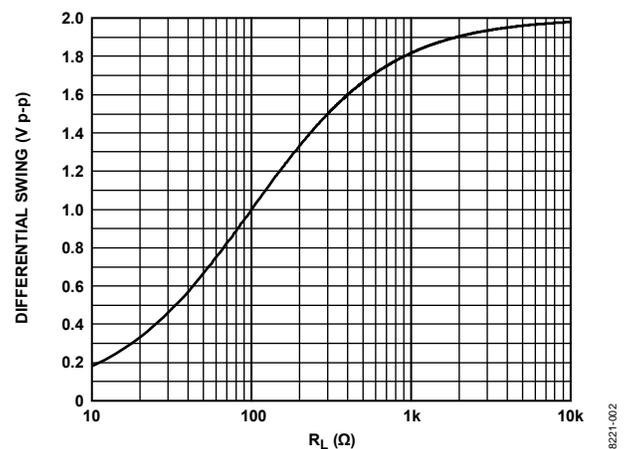


Figure 2. Relationship Between the AC Swing Limiting Resistor and the Peak-to-Peak Voltage Swing with 50 Ω Bias Setting Resistors

It is generally necessary to low-pass filter the DAC outputs to remove image frequencies when driving a modulator. This interface lends itself well to the introduction of such a filter. Insert the filter between the dc bias setting resistors and the ac swing limiting resistor to establish the input and output impedances for the filter.

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REVISION HISTORY

9/2016—Rev. A to Rev. B

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| Document Title Changed from CN-0018 to AN-1422 | Universal |
| Changes to Circuit Description Section | 1 |
| Changes to Common Variations Section | 2 |

5/2009—Rev. 0 to Rev. A

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| Updated Format | Universal |
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10/2008—Revision 0: Initial Version

Figure 3 shows a simulated filter example with a third-order elliptical filter and a 3 dB frequency of 3 MHz. Matching input and output impedances make the filter design easier; therefore, the shunt resistor is 100 Ω , producing an ac swing of 1 V p-p differential for a 0 mA to 20 mA DAC full-scale output current. In a practical application, the use of standard value components, along with the input impedance of the I/Q modulator (2900 k Ω in parallel with a few picofarads of input capacitance), slightly changes the frequency response of this circuit.

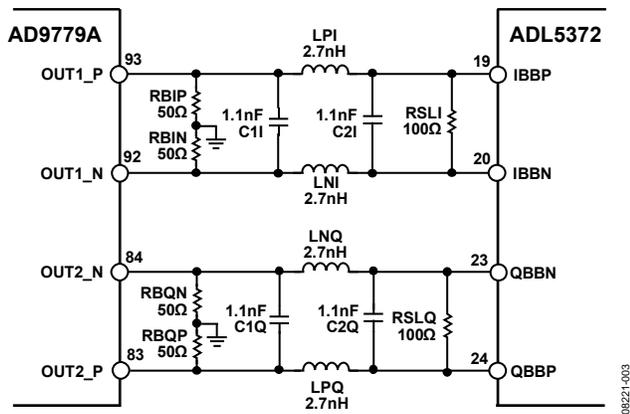


Figure 3. DAC Modulator Interface with 3 MHz Third-Order, Low-Pass Filter
(Calculated Component Values)

Connect all of the power supply pins of the ADL5372 to the same 5 V source. Tie together and decouple the adjacent pins of the same name to a large area ground plane with a 0.1 μ F capacitor. Locate these capacitors as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

Tie the COM1, COM2, COM3, and COM4 pins to the same ground plane through low impedance paths. In addition, solder the exposed paddle on the underside of the package to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, stitch them together with nine vias under the exposed paddle. The AN-772 Application Note discusses the thermal and electrical grounding of the LFCSP in greater detail.

COMMON VARIATIONS

The interface described can interface with any TxDAC converter with ground referenced, 0 mA to 20 mA output currents to any I/Q modulator with a 0.5 V input bias level. For zero-IF applications, the AD9783 dual DAC provides an LVDS interface, while the CMOS driven AD9788 dual DAC can generate a fine resolution complex IF input to the I/Q modulator. The ADL5370/ADL5371/ADL5372/ADL5373 family of I/Q modulators provide narrow-band operation with high output 1 dB compression point and output third-order intercept (IP3), whereas the ADL5385 provides broadband high performance operation from 400 MHz to 6 GHz. The ADL5385 I/Q modulator uses a $2 \times$ LO and operates from 50 MHz to 2.2 GHz.

REFERENCES

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