# IS32LT3141B

## SINGLE CHANNEL 450mA LED DRIVER WITH ONEWIRE SERIAL BUS AND FAULT DETECTION

**December 2021**

### GENERAL DESCRIPTION

The IS32LT3141B is an automotive-grade high-side programmable current regulator consisting of a single output channel capable of 450mA. An external resistor sets the current level for the single-channel current source. It supports a Onewire serial BUS interface to implement output on/off control. A resistor divider circuit can be used on the UV pin to set an external VCC under-voltage lockout threshold for LED string open fault detection. In addition, the IS32LT3141B integrates fault protection for a LED string open/short, output overcurrent (not reported), and over-temperature condition for robust operation. Detection of these failures is reported by the FAULTB pin. When a fault is detected the device will disable itself and output an active low open drain signal. Multiple devices can have their FAULTB pins connected to create a "one-fail-all-fail" condition.

The IS32LT3141B is targeted at the automotive market with end applications to include interior and exterior lighting. For 12V automotive applications, the low dropout driver can support one to several LEDs on the output channel. The device is offered in a small thermally enhanced SOP-8-EP package.

### FEATURES

- Wide input voltage range, 4.5V to 40V
- Onewire serial BUS Interface to control LED on/off
  - ✓ Up to 100kbps data transfer rate
  - ✓ Cascaded devices up to 30 devices
- Single-channel, sources up to 450mA
- High-side external resister sets source current
- ±8% current accuracy over -40°C ~ +150°C
- Low headroom voltage, max 700mV at 150mA
- Fault protection with open-drain flag output:
  - ✓ LED string open/short
  - ✓ Output overcurrent (not reported)
  - ✓ Thermal shutdown
- Shared fault flag for multiple device operation to comply with "one-fail-all-fail" function
- AEC-Q100 Qualified
- Operating temperature range from -40°C ~ +150°C

### APPLICATIONS

- Automotive interior/exterior lighting:
  - Sequential turn signal light
  - Rear lamp
  - Front lamp

### TYPICAL APPLICATION CIRCUIT

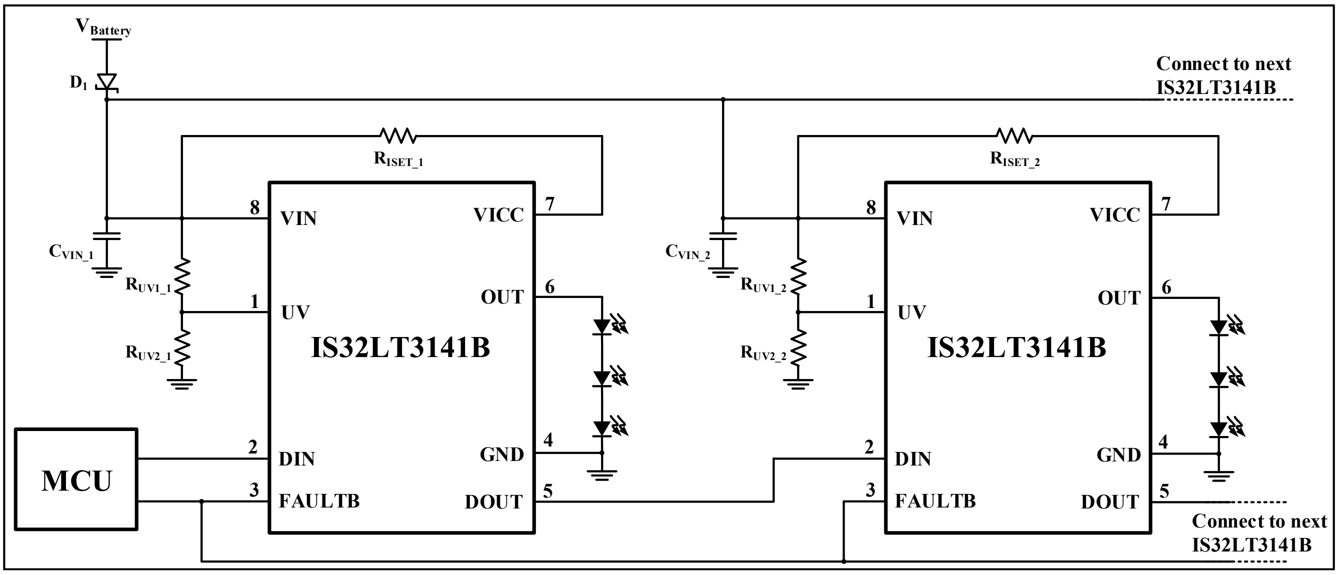
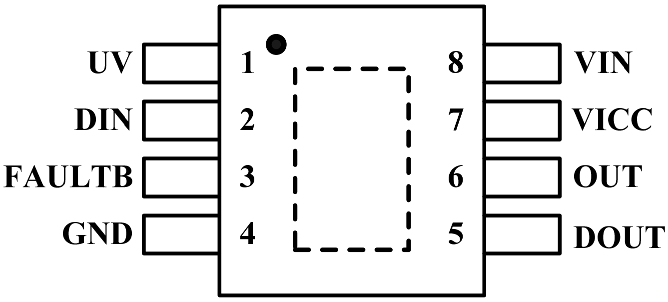



**Figure 1** Typical Application Circuit

**Note 1:** The current sense resistor $R_{ISET}$ must be placed as close as possible to VIN and VICC pins on the PCB layout to avoid noise interference.

## PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---|---|
| SOP-8-EP |  |

## PIN DESCRIPTION

| No. | Pin | Description |
|---|---|---|
| 1 | UV | External under voltage lockout threshold setting for LED string open fault detection. Pull low will disable the LED open fault detection. If unused, it must be connected to VIN pin via a resistor (recommended value is 10kΩ). |
| 2 | DIN | Onewire serial BUS serial data input. It is internally pulled up to 3.3V (Typ.) LDO by 50kΩ resistor. |
| 3 | FAULTB | Open drain I/O diagnostic pin. Active low output driven by the device when it detects a fault condition. This pin will accept an externally generated FAULTB signal to disable the device output to satisfy the “one fail all fail” function. This pin is internally pulled up to internal 4.5V (Typ.) LDO by a 50kΩ (Typ.) resistor. |
| 4 | GND | Ground. |
| 5 | DOUT | Onewire serial BUS serial data output. If unused, leave it floating. |
| 6 | OUT | Output current source channel. |
| 7 | VICC | Current input and current sense pin. |
| 8 | VIN | Power supply input and current sense pin. |
| | Thermal Pad | MUST be electrically connected to large GND plane for better thermal dissipation. |

## ORDERING INFORMATION
**Automotive Range: -40°C to +125°C**

| Order Part No. | Package | QTY/Reel |
|---|---|---|
| IS32LT3141B-GRLA3-TR | SOP-8-EP, Lead-free | 2500 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Voltage on UV, FAULTB, OUT, VICC, VIN pins | -0.3V ~ +45V |
| Voltage on DIN, DOUT pins | -0.3V ~ +22V |
| VIN pin to VICC pin voltage, $V_{IN}$ - $V_{VICC}$ | -0.3V ~ +1V |
| Operating temperature, $T_A$=$T_J$ | -40°C ~ +150°C |
| Maximum continuous junction temperature, $T_{J(MAX)}$ | +150°C |
| Storage temperature range, $T_{STG}$ | -65°C ~ +150°C |
| Package thermal resistance, junction to ambient (4-layer standard test PCB based on JEDEC standard), $\theta_{JA}$ | 43.6°C/W |
| Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JEDEC standard), $\theta_{JP}$ | 1.39°C/W |
| Maximum power dissipation, $P_{DMAX}$ | 2.87W |
| ESD (HBM)<br>ESD (CDM) | ±2kV<br>±750V |

**Note 2:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$T_J$= $T_A$= -40°C ~ +150°C, $V_{IN}$= 12V, the detail refer to each condition description, unless otherwise noted. Typical values are at $T_J$= $T_A$= 25°C (Note 3).

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power Up Parameter** | | | | | | |
| $V_{IN}$ | Supply voltage range | | 4.5 | | 40 | V |
| $V_{UVLO\_R}$ | VIN under voltage lockout rising threshold | | | 3.2 | 4.0 | V |
| $V_{UVLO\_F}$ | VIN under voltage lockout falling threshold | | 2.2 | 3.0 | | V |
| $I_{IN}$ | VIN quiescent current | No fault conditions | 0.8 | 1.1 | 1.4 | mA |
| $I_{IN\_FLT}$ | VIN supply current in fault condition | $V_{UV}$= High,<br>FAULTB externally pulled low | 0.9 | 1.2 | 1.5 | mA |
| **Channel Parameter** | | | | | | |
| $I_{OUT\_R}$ | Channel output current range | 100% duty cycle | -450 | | -4 | mA |
| $V_{SENSE}$ | Current sense voltage ($V_{IN}$-$V_{ICC}$) | $V_{IN}$= 4.5V to 18V, $T_J$= $T_A$= 25°C | 95 | 100 | 105 | mV |
| | | $V_{IN}$= 4.5V to 18V,<br>$T_J$= $T_A$= -40°C ~ +150°C | 92 | 100 | 108 | mV |
| $V_{HR\_MIN}$ | Minimum headroom voltage, from VIN to OUT ($V_{SENSE}$ included) | $I_{OUT}$= -10mA | | 120 | 150 | mV |
| | | $I_{OUT}$= -70mA | | 250 | 400 | mV |
| | | $I_{OUT}$= -150mA | | 430 | 700 | mV |
| | | $I_{OUT}$= -300mA | | 800 | 1300 | mV |
| $I_{OUT\_L}$ | Output limit current | VIN shorted to VICC,$V_{HR}$=3V | | -600 | | mA |
| $I_{LEAK}$ | Channel leakage current | $V_{OUT}$= 0V | | | 3 | μA |

## ELECTRICAL CHARACTERISTICS (CONTINUE)

$T_J$= $T_A$= -40°C ~ +150°C, $V_{IN}$= 12V, the detail refer to each condition description, unless otherwise noted. Typical values are at $T_J$= $T_A$= 25°C (Note 3).

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{SL}$ | Current rising/falling slew time | Enabled/disabled by commands, current rise/fall between 10%~90%, $I_{OUT}$= -300mA | 8 | 16 | 24 | μs |
| **Fault Protect Parameter** | | | | | | |
| $t_{FD\_DT}$ | Fault detect deglitch time | *Fault must be present at least this long to trigger the fault detect | 70 | 130 | 190 | μs |
| $t_{FD\_RL}$ | Fault release deglitch time | | 30 | 60 | 90 | μs |
| $V_{FAULTB\_PU}$ | FAULTB pin internally pull-up voltage | | 4 | | 5.5 | V |
| $R_{FAULTB}$ | FAULTB pin pull-up resistor | | | 50 | | kΩ |
| $V_{FAULTB\_PD}$ | FAULTB pin externally pull-down voltage | Sink current= 5mA | | 0.2 | 0.4 | V |
| $V_{FAULTB\_IH}$ | FAULTB pin input high enable threshold | | 2 | | | V |
| $V_{FAULTB\_IL}$ | FAULTB pin input low disable threshold | | | | 0.7 | V |
| $V_{SCD\_R}$ | OUT pin short to GND rising threshold | Measured at OUT pin | 1.1 | 1.2 | 1.3 | V |
| $V_{SCD\_F}$ | OUT pin short to GND falling threshold | Measured at OUT pin | 0.82 | 0.865 | 0.91 | V |
| $V_{OD\_R}$ | OUT pin open rising threshold | Measured at ($V_{VICC}$-$V_{OUT}$) | 70 | 120 | 160 | mV |
| $V_{OD\_F}$ | OUT pin open falling threshold | Measured at ($V_{VICC}$-$V_{OUT}$) | 250 | 320 | 400 | mV |
| $I_{RTR}$ | Output retry current in fault modes | $V_{OUT}$= 0V | -1.6 | -1 | -0.6 | mA |
| $T_{SD}$ | Thermal shutdown threshold | (Note 4) | | 175 | | °C |
| $T_{HY}$ | Over-temperature hysteresis | (Note 4) | | 25 | | °C |
| **Logic Input** | | | | | | |
| $V_{UV\_IH}$ | UV input rising threshold | | 1.14 | 1.20 | 1.3 | V |
| $V_{UV\_IL}$ | UV input falling threshold | | 1.045 | 1.1 | 1.155 | V |

## ELECTRICAL CHARACTERISTICS (CONTINUE)

$T_J$= $T_A$= -40°C ~ +150°C, $V_{IN}$= 12V, the detail refer to each condition description, unless otherwise noted. Typical values are at $T_J$= $T_A$ = 25°C (Note 3).

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Onewire Serial BUS** | | | | | | |
| $V_{IH\_DIN}$ | DIN pin input logic high voltage | | 2.0 | | | V |
| $V_{IL\_DIN}$ | DIN pin input logic low voltage | | | | 0.7 | V |
| $R_{PU\_DIN}$ | DIN pin internal pull-up resistor | | | 50 | | kΩ |
| $V_{DOUT\_H}$ | DOUT output high voltage | $I_{DOUT}$= -200μA | 3.1 | 3.3 | 3.5 | V |
| $V_{DOUT\_L}$ | DOUT output low voltage | $I_{DOUT}$= 1mA | | | 0.4 | V |
| $T_C$ | DIN input signal period time | | 10 | | 100 | μs |
| $D_{DIN}$ | Duty cycle range of $T_C$ | For $T_C$ including both of logic high and logic low, $t_H/T_C$ | 35 | 50 | 65 | % |
| $t_{PLH}$ | DIN to DOUT low to high propagation delay time | $C_{DOUT}$=15pF, $t_R$=$t_F$=3ns | | 50 | | ns |
| $t_{PHL}$ | DIN to DOUT high to low propagation delay time | $C_{DOUT}$=15pF, $t_R$=$t_F$=3ns | | 50 | | ns |
| $t_{RESET}$ | "RESET" signal time | | 12 | | | ms |
| $t_{SYNC\_TO}$ | "Start and Sync" signal time-out time | | | 9 | 14 | ms |

**Note 3:** Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

**Note 4:** Guaranteed by design.

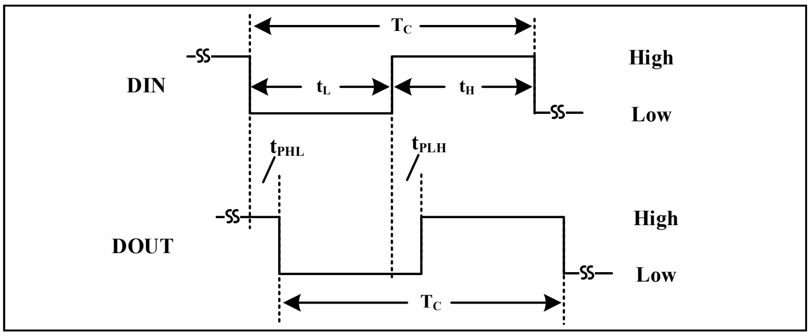
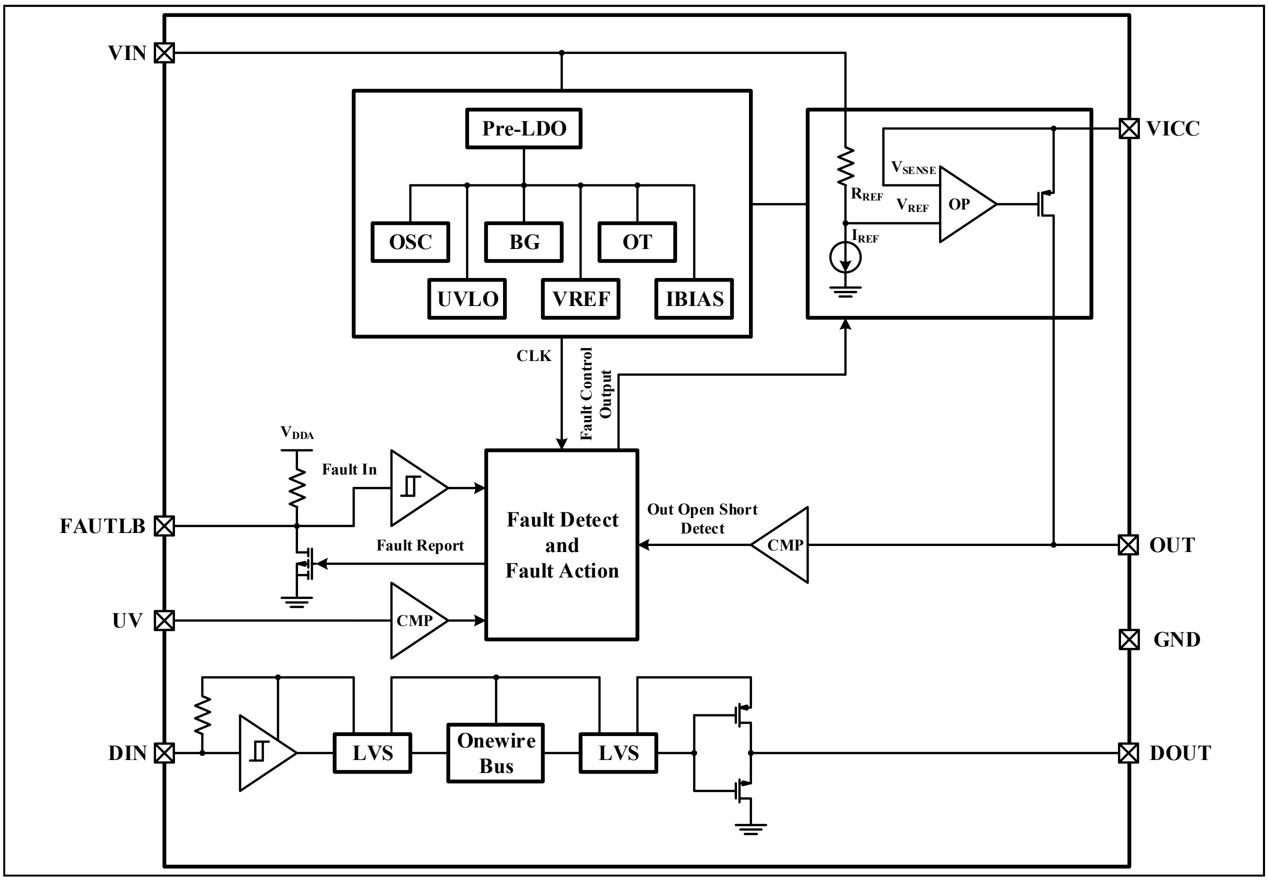



**Figure 2** Onewire BUS Timming

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL PERFORMANCE CHARACTERISTICS

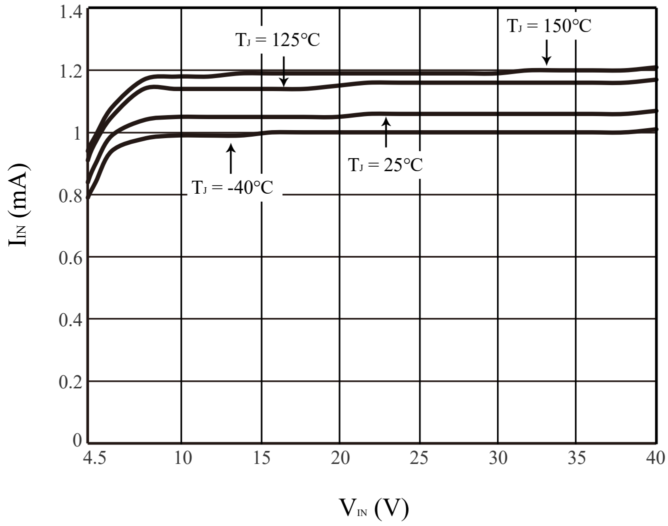



**Figure 3** $I_{IN}$ vs. $V_{IN}$

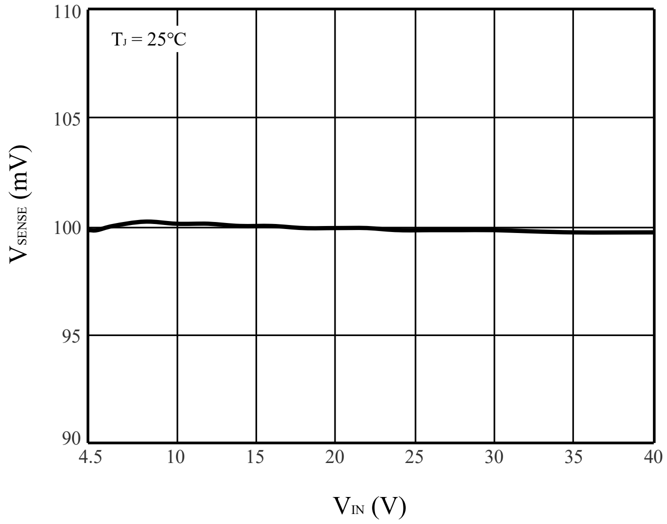



**Figure 4** $V_{SENSE}$ vs. $V_{IN}$

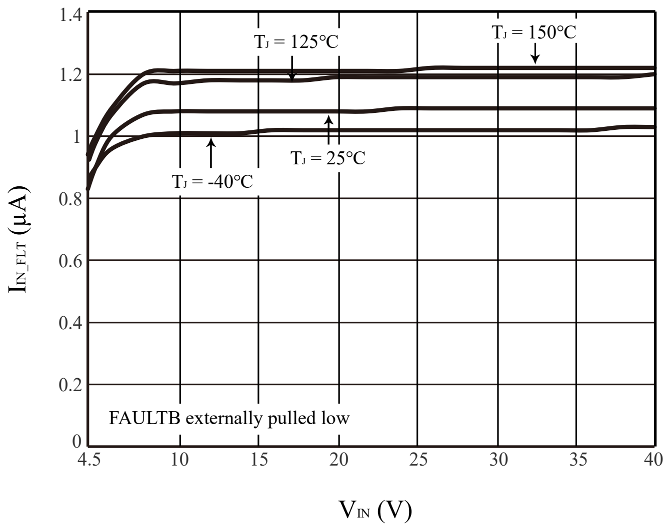



**Figure 5** $I_{IN\_FLT}$ vs. $V_{IN}$

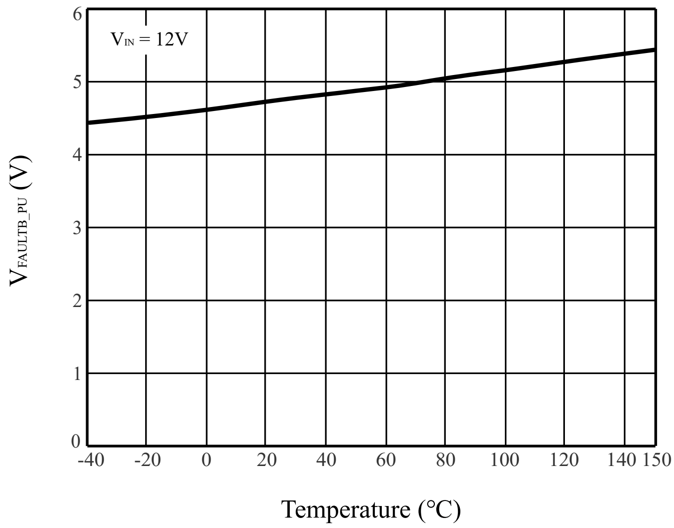



**Figure 6** $V_{FAULTB\_PU}$ vs. $T_J$

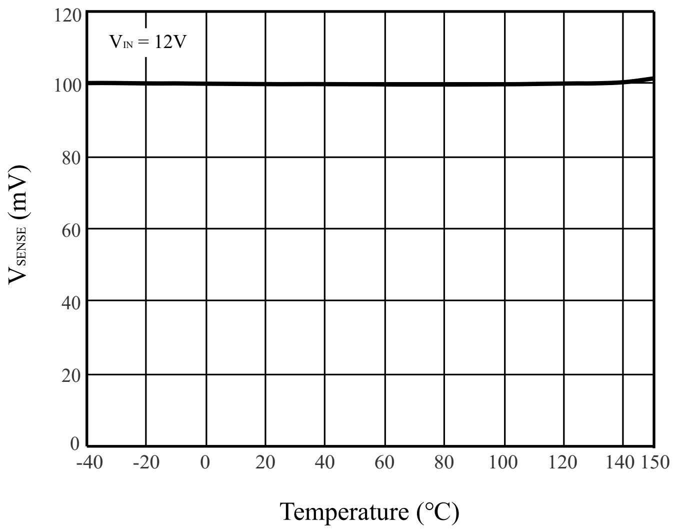



**Figure 7** $V_{SENSE}$ vs. $T_J$

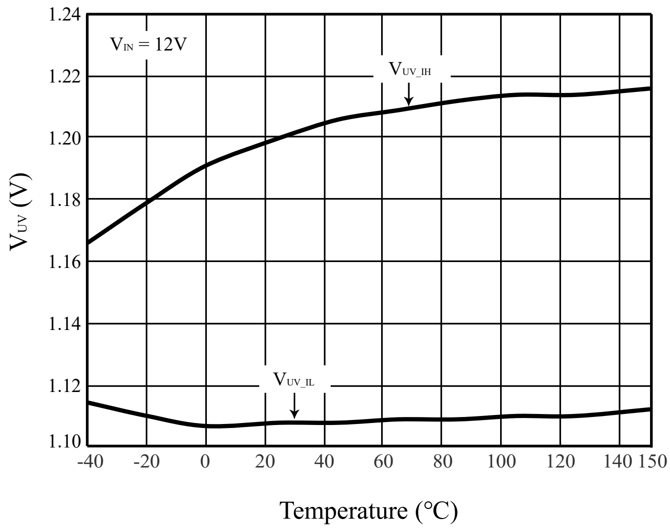



**Figure 8** $V_{UV}$ vs. $T_J$

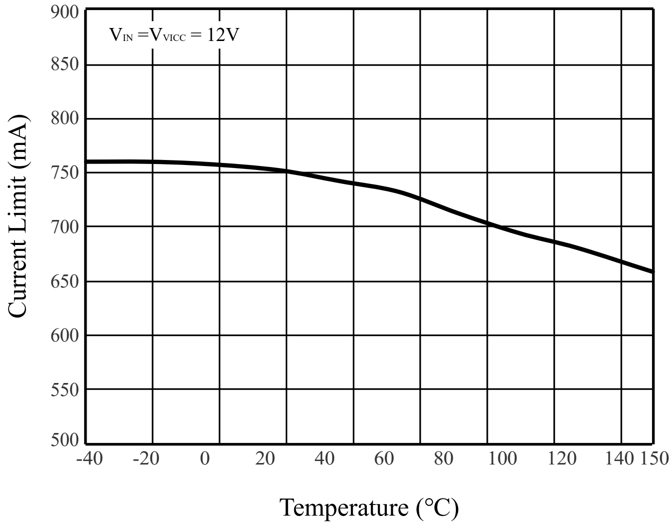



**Figure 9** $I_{OUT\_L}$ vs. $T_J$

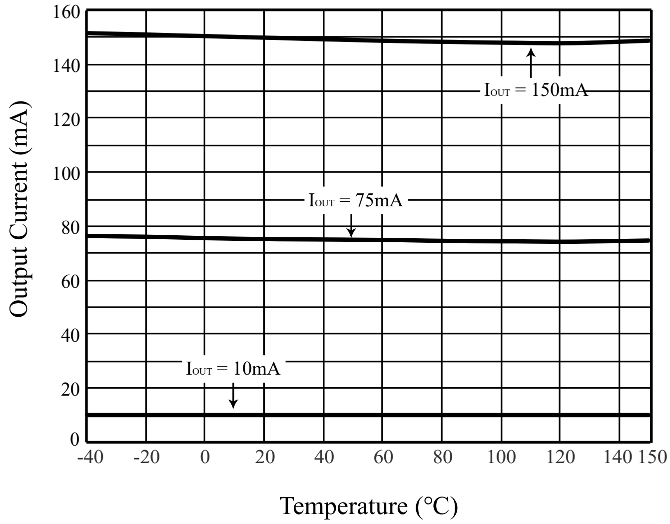



**Figure 10** $I_{OUT}$ vs. $T_J$

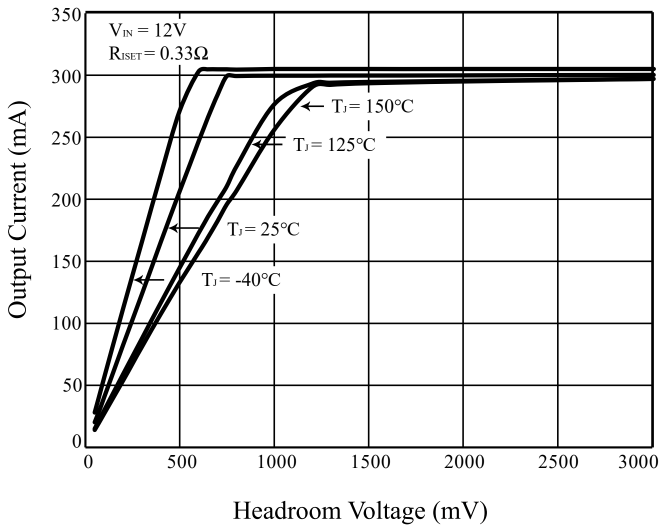



**Figure 11** Output Current vs. Headroom Voltage

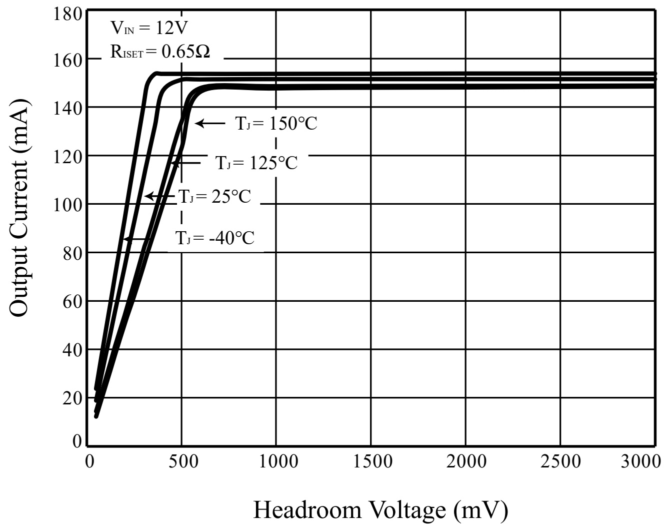



**Figure 12** Output Current vs. Headroom Voltage

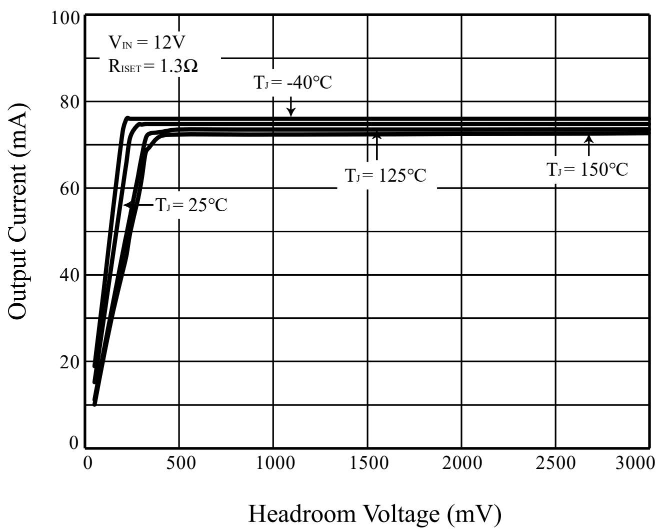



**Figure 13** Output Current vs. Headroom Voltage

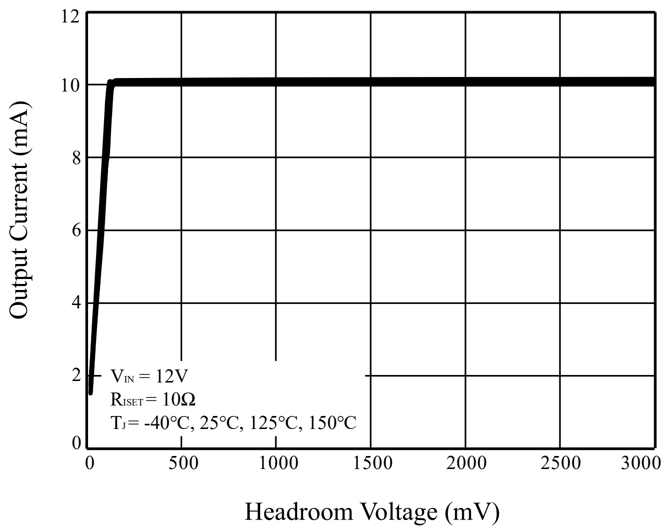



**Figure 14** Output Current vs. Headroom Voltage

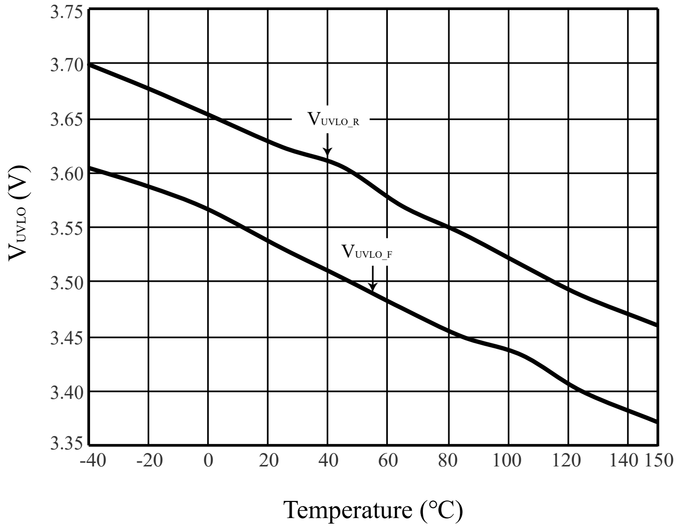



**Figure 15** $V_{UVLO}$ vs. $T_J$

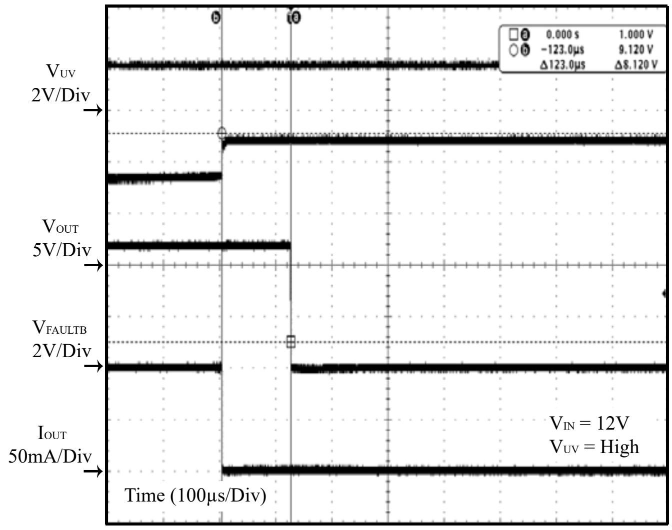



**Figure 16** Output Open

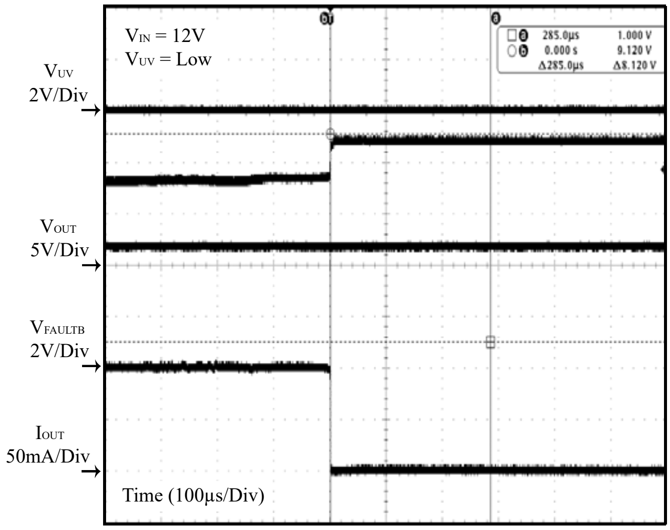



**Figure 17** Output Open

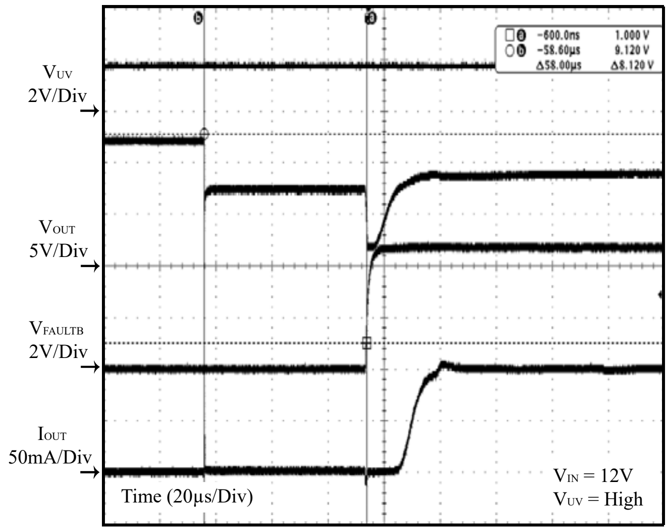



**Figure 18** Output Open Fault Remove

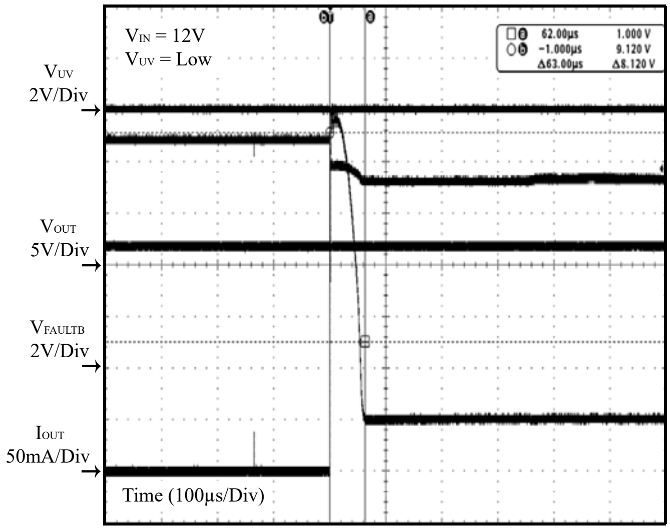



**Figure 19** Output Open Fault Remove

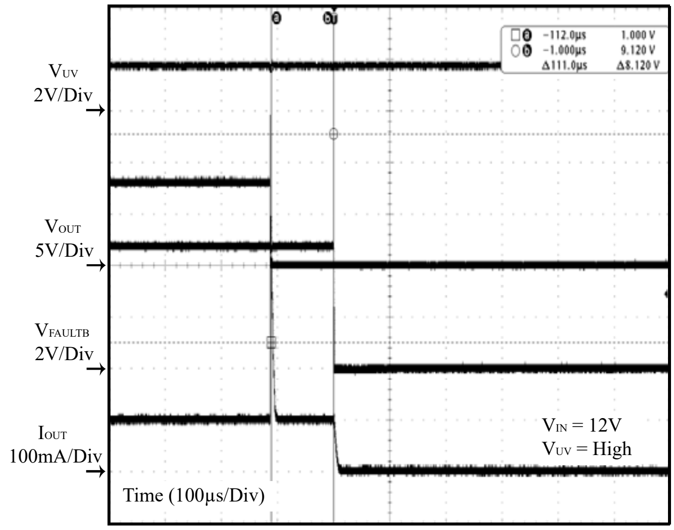



**Figure 20** Output Short

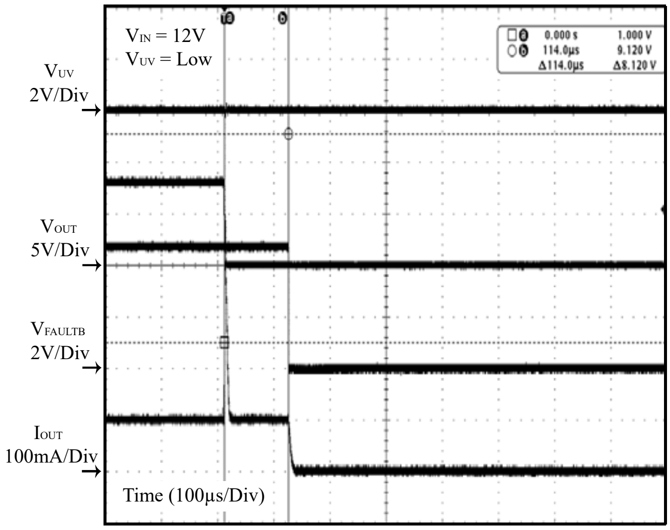



**Figure 21** Output Short

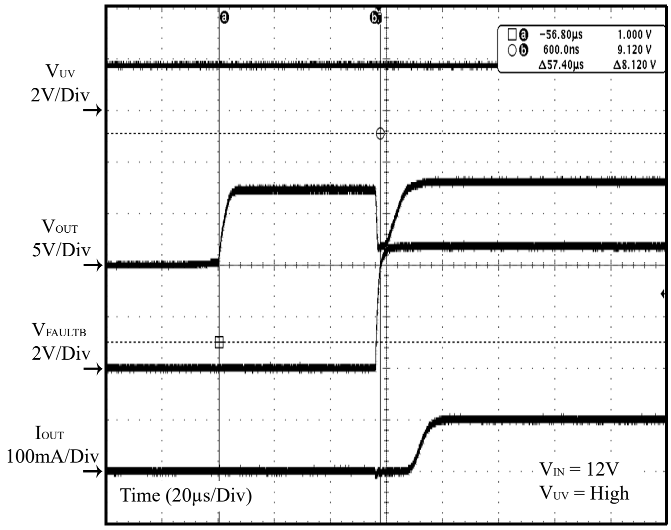



**Figure 22** Output Short Fault Remove

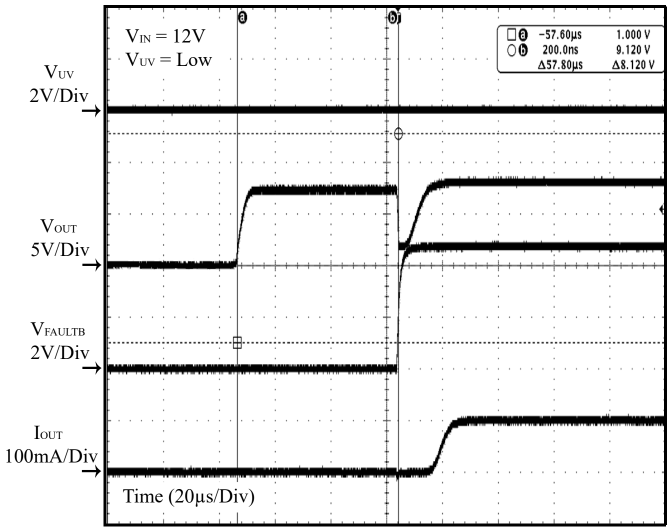



**Figure 23** Output Short Fault Remove

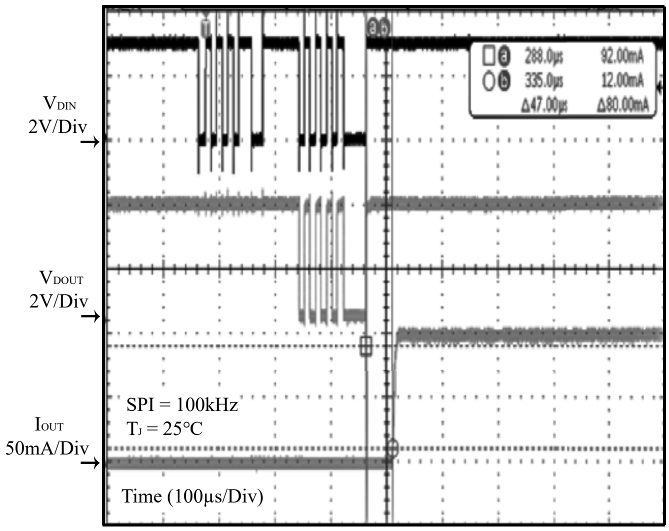



**Figure 24** Onewire Bus – “ON” and “LATCH” Control

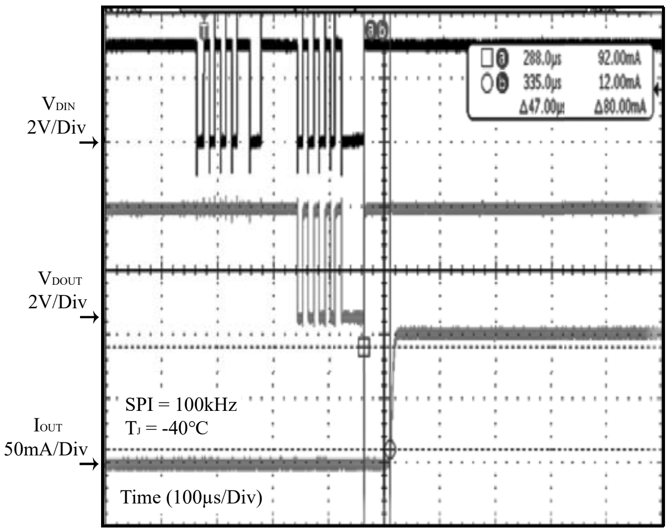



**Figure 25** Onewire Bus – “ON” and “LATCH” Control

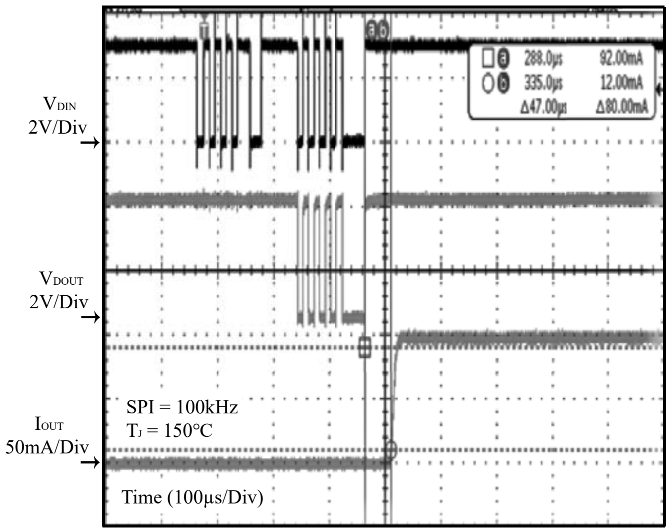



**Figure 26** Onewire Bus – “ON” and “LATCH” Control

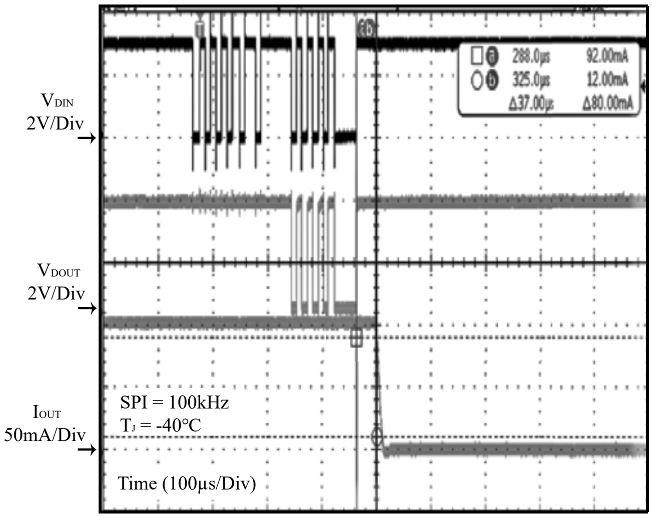



**Figure 27** Onewire Bus – “OFF” and “LATCH” Control

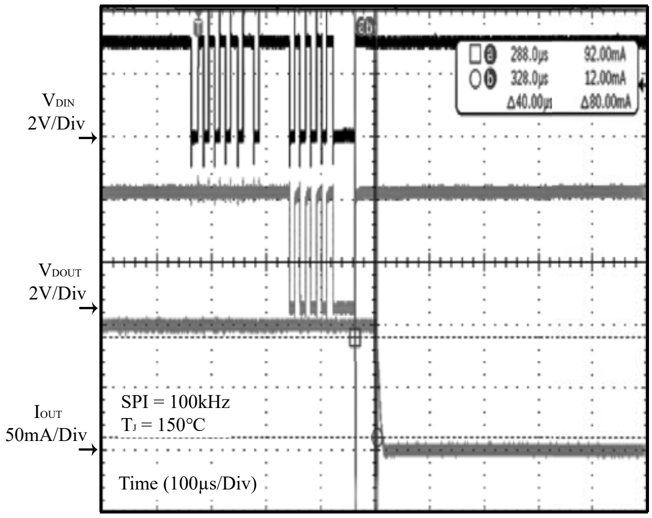



**Figure 28** Onewire Bus – “OFF” and “LATCH” Control

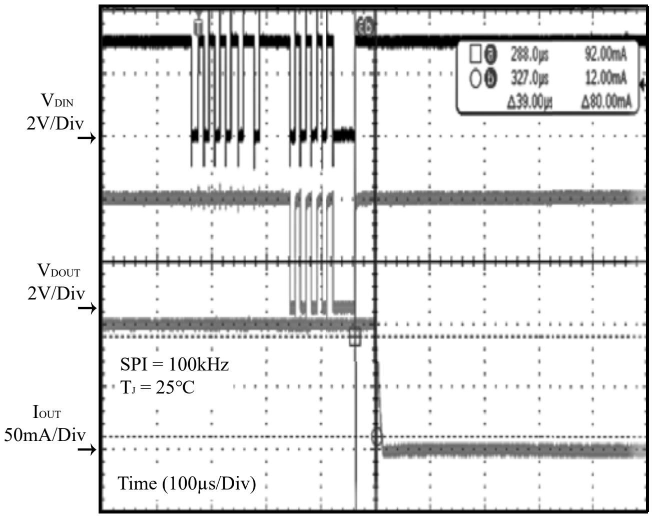



**Figure 29** Onewire Bus – “OFF” and “LATCH” Control

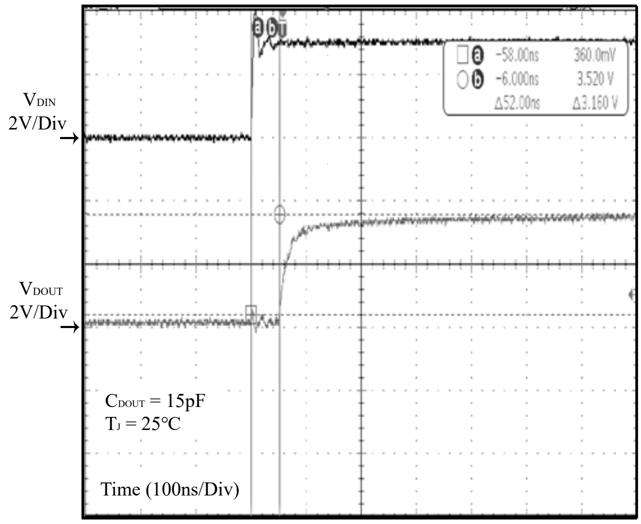



**Figure 30** DIN and DOUT Propagation Delay Time

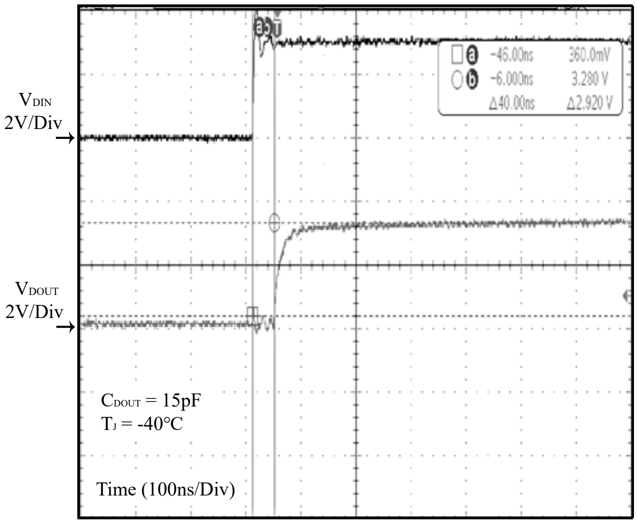



**Figure 31** DIN and DOUT Propagation Delay Time

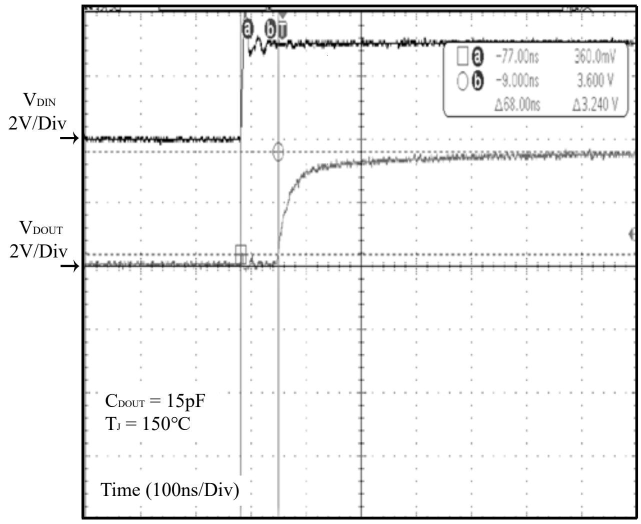



**Figure 32** DIN and DOUT Propagation Delay Time

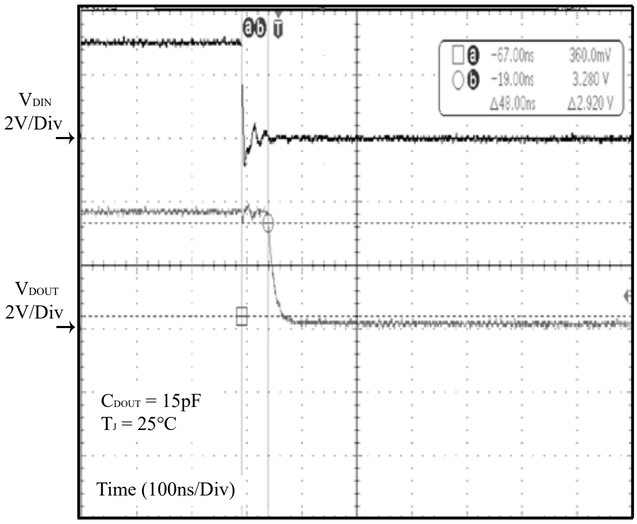



**Figure 33** DIN and DOUT Propagation Delay Time

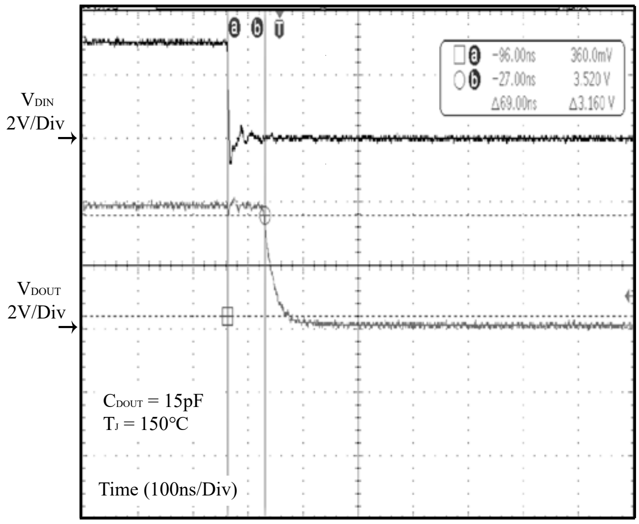



**Figure 34** DIN and DOUT Propagation Delay Time

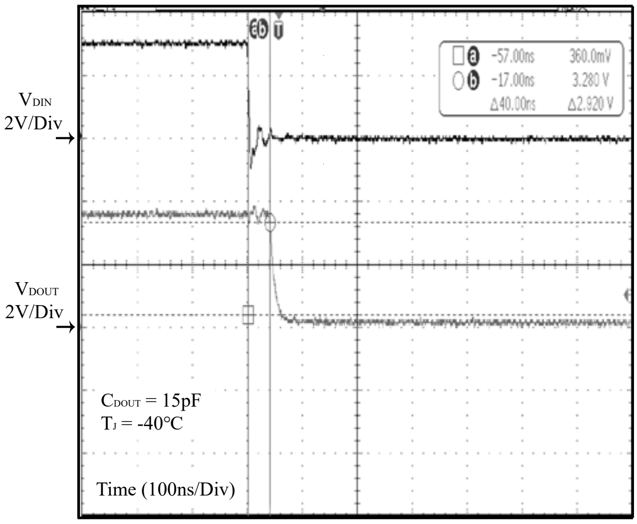



**Figure 35** DIN and DOUT Propagation Delay Time

## APPLICATION INFORMATION

The IS32LT3141B is a programmable linear current source capable of regulating a constant current up to 450mA. A single resistor $R_{ISET}$ is connected across the VIN and VICC pins to set the output current value. The current flows from the power supply through the $R_{ISET}$ resistor into the VICC pin and internal current source and out from OUT pin to LED string. The device senses the voltage drop on the $R_{ISET}$ resistor and an internal regulation loop drives the output current source to regulate the voltage drop on the $R_{ISET}$ resistor at $V_{SENSE}$.

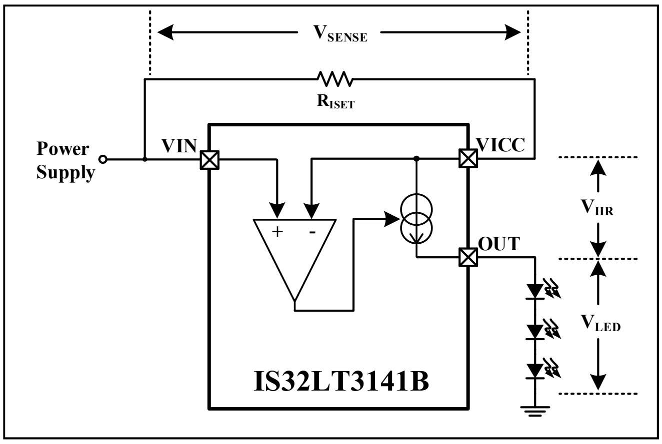



**Figure 36** Constant Current Regulation

## OUTPUT CURRENT SETTING

The regulated maximum LED current is set by the current sense resistor $R_{ISET}$. The $R_{ISET}$ resistor value can be calculated using the following equation:

$$R_{ISET} = \frac{V_{SENSE}}{I_{LED}} \quad (1)$$

Where $I_{LED}$ is the desired LED current in Amp and $R_{ISET}$ is in Ω. $V_{SENSE}$ is current sense voltage, 0.1V typical.

It is recommend that $R_{ISET}$ be a 1% accuracy resistor with good temperature characteristic to ensure stable and precise output current. On the PCB layout, this resistor must be placed as close to VIN pin and VICC pin as possible to avoid noise interference.

When the desired current is high, the power rating also should be considered. The maximum power dissipation on the $R_{ISET}$ resistor is calculated by:

$$P_{RISET} = V_{SENSE} \times I_{LED} \quad (2)$$

A single high wattage resistor or several small wattage resistors in parallel can be used to sustain the power dissipation.

The device is protected from an output overcurrent condition caused by $R_{ISET}$ resistor. The output current is limited to an $I_{OUT\_L}$ value of -600mA should a low value resistor be connected to VIN and VICC pins.

## UNDER VOLTAGE LOCKOUT (UVLO)

IS32LT3141B features an under voltage lockout (UVLO) function on the VIN pin to prevent misoperation at low input voltages. The UVLO threshold is an internally fixed value and cannot be adjusted. The device is enabled when the $V_{IN}$ voltage exceeds $V_{UVLO\_R}$ (Typ. 3.2V), and disabled when the $V_{IN}$ voltage falls below $V_{UVLO\_F}$ (Typ. 3.0V).

## ONEWIRE SERIAL BUS

An external MCU can easily control output ON/OFF of multiple IS32LT3141B slaves through a onewire serial BUS. As shown in Figure 41. The protocal uses a single data line with cascaded connection between slaves for data transmission. A clock is not required as each slave is clocked by an internal oscillator which is synchronized in-coming command frame from the MCU. Therefore, this protocol significantly simplifies the MCU I/O requirement. A single push-pull I/O can control upto 30 slaves. The onewire serial BUS implements simplex communication. The MCU initiates all transfers on the data line. Transfer of data can only be from the MCU to the slaves and the achievable data rate ($1/T_C$) range is 10kbps to 100kbps. The idle state of the onewire serial BUS is logic high.

There only four types of command frames possible on the data line:

**Table 1 Onewire Serial BUS Command**

| Command | Function |
|---|---|
| ON | Stores ON data into internal data buffer and closes path switch |
| OFF | Stores OFF data into internal data buffer and closes path switch |
| LATCH | Latch ON/OFF data from internal data buffer to output stage (output current source) and opens path switch |
| RESET | Reset state machine to standby mode and opens path switch |

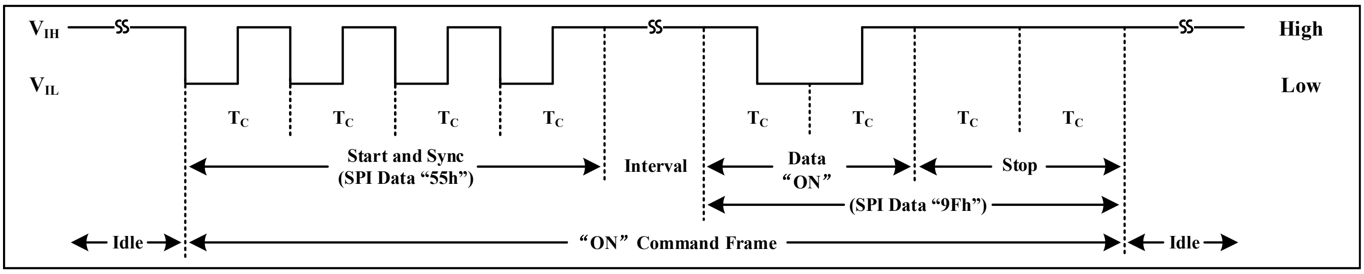



**Figure 37** Onewire Serial BUS "ON" Command Frame

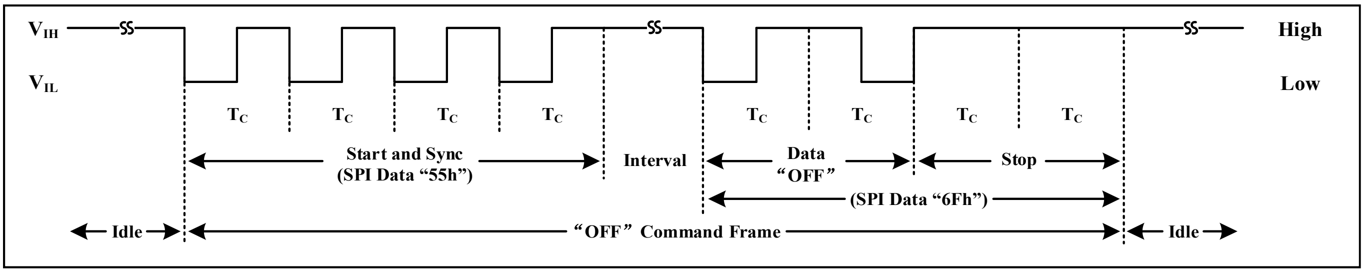



**Figure 38** Onewire Serial BUS "OFF" Command Frame

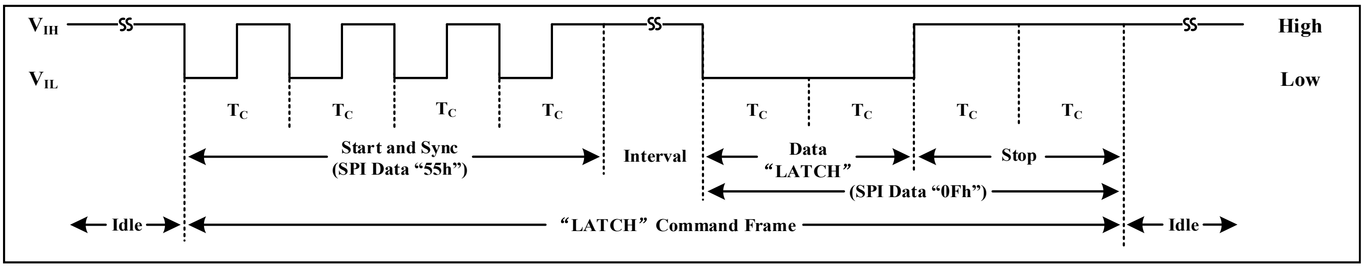



**Figure 39** Onewire Serial BUS "LATCH" Command Frame

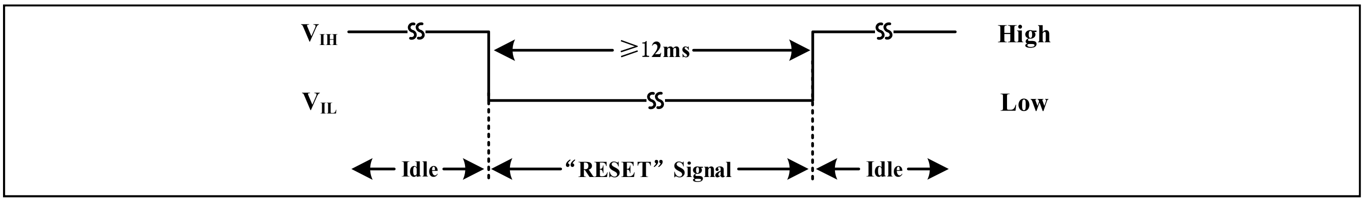



**Figure 40** Onewire Serial BUS "RESET" Signal

The frame of "ON", "OFF" and "LATCH" command consists of the "Start and Sync" signal, the interval time, the "Data" signal and the "Stop" signal. The "Start and Sync" signal is 4x$T_C$ which starts the command frame transmission and synchronizes the transmission data rate to the slaves. The synchronized data rate will be stored in the slaves until the next "Start and Sync" signal. A logic high interval time no longer than 10ms is allowed between the "Start and Sync" signal and "Data" signal. Both the "Data" and "Stop" signals are 2x$T_C$ and their data rate must be identical with the "Start and Sync" signal. The "Stop" signal ends the command frame transmission.

In a typical application, the MOSI line of a common SPI hardware interface with MODE 3 (CPOL=High and CPHA =2 Edge) can be used for "ON", "OFF" and "LATCH" command frames transmission, and leave the other lines (CS, SCK and MISO) of the SPI interface floating. The data rate of the SPI interface should be set at 2/$T_C$. Then the "Start and Sync" signal can be transferred by one byte of SPI command. The "Data" signal and the "Stop" signal can be transferred by another byte of SPI command. As Table 2.

**Table 2 SPI Data for Onewire Serial BUS Command**

| Onewire Serial BUS Command | SPI MOSI Data (HEX) | |
|---|---|---|
| | Start and Sync | Data and Stop |
| ON | 55h | 9Fh |
| OFF | 55h | 6Fh |
| LATCH | 55h | 0Fh |

After SPI interface initialization, the MOSI line may be in a logic low state. Please force the SPI to send a "FFh" data after to get a logic high for the onewire serial BUS idle state, See Figure 43 and 44 program flow chart.

Driving the onewire serial BUS low for a period of at least 12ms results in a "RESET" signal which resets the state machine of IS32LT3141B to an initial known-good standby mode for receiving command frames. The IS32LT3141B immediately aborts any command frame receiving action and opens the internal path switch. After power up, the MCU must send a "RESET" signal to initialize the onewire serial BUS. Note that, since the MOSI line is not able to send a ≥12ms low pulse, the MOSI pin should be confirgured as push-pull I/O mode to send the "RESET" signal.

As shown in Figure 41. There is a path switch and a data buffer inside each IS32LT3141B device. The path switch is used to connect the DIN to the DOUT. After power up, all IS32LT3141B slaves are in standby mode for command receiving, their path switches in open state and their output stage (output current source) in off state.

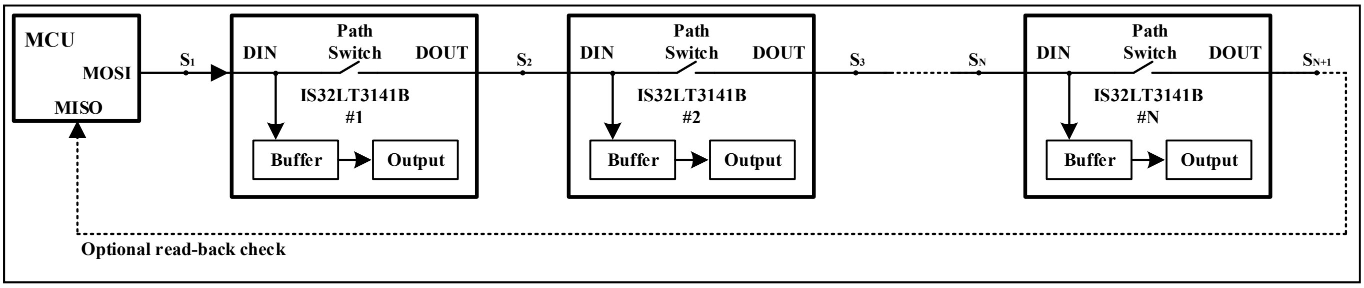



**Figure 41** Onewire Serial BUS Connection

Figure 42 shows command frames transmission process. Due to DOUT being disconnected from its corresponding DIN, when the MCU sends out first "ON" or "OFF" command frame, only the #1 slave closest to the MCU can recieve the command frame. If the command frame is valid, the #1 slave will store the received command into its internal data buffer and close its path switch. After that, this #1 slave will ignore the next "ON" or "OFF" command frames from the BUS. When the MCU sends out the next "ON" or "OFF" command frame, the #2 slave is able to recieve this command frame through the #1 slave. The #2 slave stores the valid command into its internal buffer and close its path switch and ignore the next "ON" or "OFF" command frames. In the same way, if all "ON" or "OFF" command frames are valid, the MCU is able to send the corresponding "ON" or "OFF" command to each slave in turn without requiring a device address. The MCU only needs to be aware of the number of devices on the onewire bus so it sends out the right number of commands.

Once the last slave storing a valid "ON" or "OFF" command, the path switches of all slaves are closed, therefore the DIN of the #1 slave is connected to the DOUT of the last slave through the path switches of all devices. The next "LATCH" command frame from the MCU is presented to all slaves and the DOUT pin of the last slave, that simoutaneously latches the "ON/OFF" command from the slaves' internal data buffers to the output stages (output current source) and then opens all the path switches. Repeating the command frame transmission progress, the MCU is able to individually control the output ON/OFF of each slave.

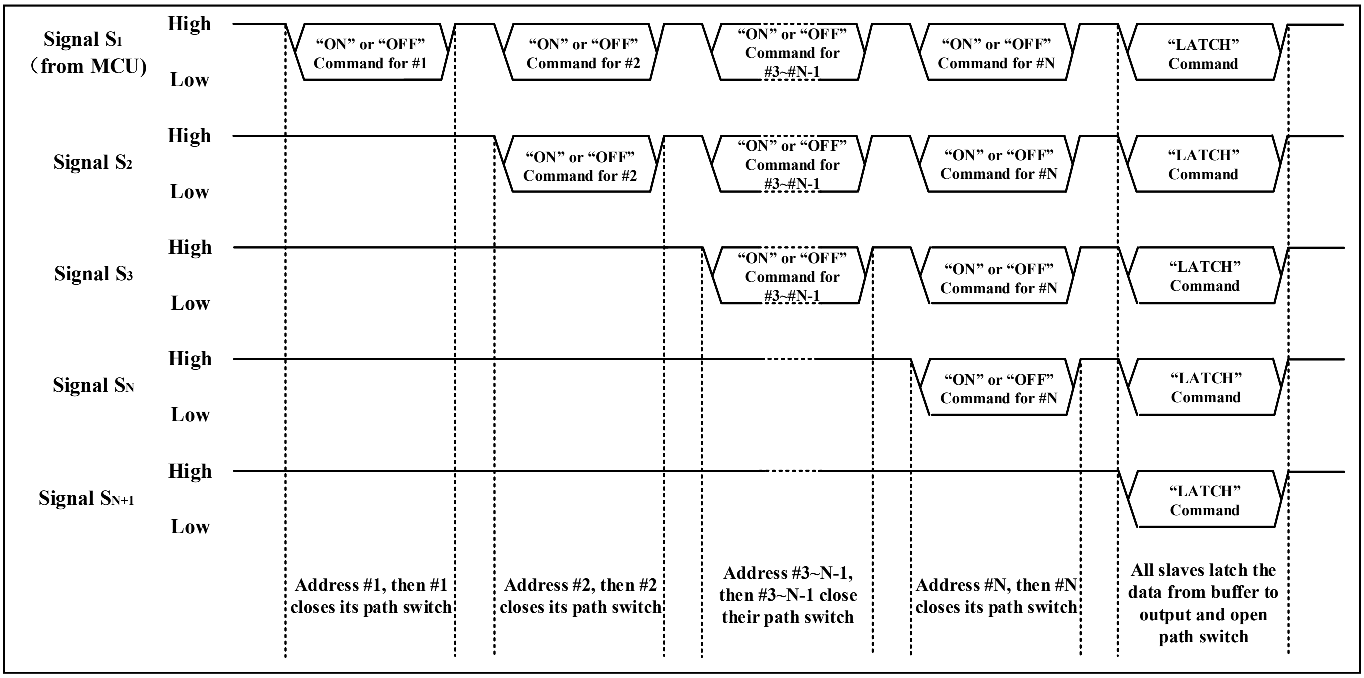



**Figure 42** Command Frames Transmission Process

During the command frame transmission process, if any "ON" or "OFF" command is invalid (such as illegal format, inconsistent data rate and so on), the corresponding slave will not store the invalid command into its data buffer so its path switch will remain in the open state. The sequential transimissions will be off. Since the onewire serial BUS is a simplex communication, the MCU cannot know whether the command frame transmission sequence was successful or not. To get a robust transmission, there are two methods to avoid this communication interruption condition:

1) Each "LATCH" command frame should be followed with a "RESET" signal which resets the onewire serial BUS and gets it ready for the next transimission process. As Figure 43 program flowchart.

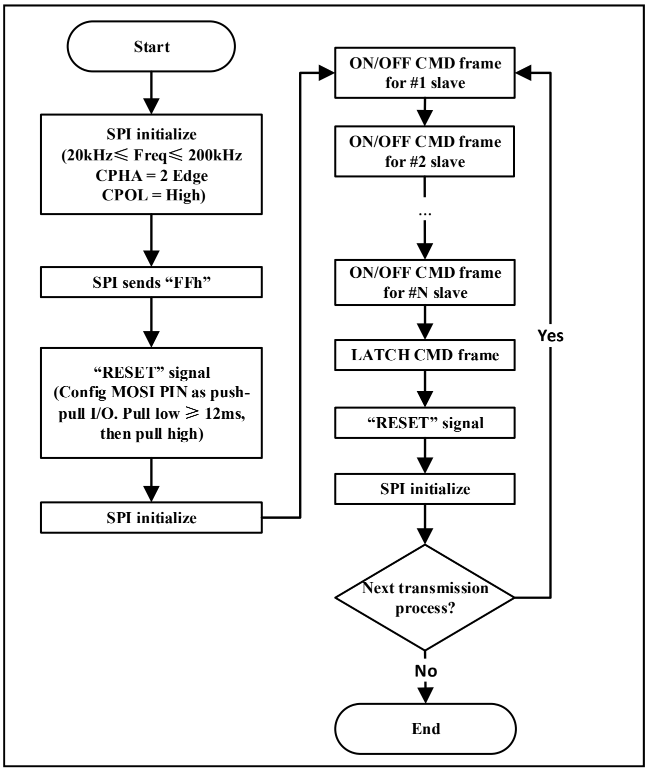



**Figure 43** Flowchart "LATCH" Follows with "RESET"

2) Connect the DOUT of the last slave to the MISO line of the SPI interface for a real-time monitoring of the last command frame. As Figure 41. During the "ON" or "OFF" command frame transmission, the DOUT of the last slave should remain in idle state (logic high). All data read by the MISO line must be "FFh". Otherwise the onewire serial BUS is in abnormal state. The MCU should abort the command frame transimission and send out a "RESET" signal to reset the onewire serial BUS. If all "ON" or "OFF" command frames are successfully transferred and the "LATCH" command frame is sent out, the data read by the MISO line must be "55h" and "0Fh", otherwise the onewire serial BUS is in abnormal state. The MCU should abort the command frames transimission and send out a "RESET" signal to reset the onewire serial BUS. As Figure 44 program flowchart.

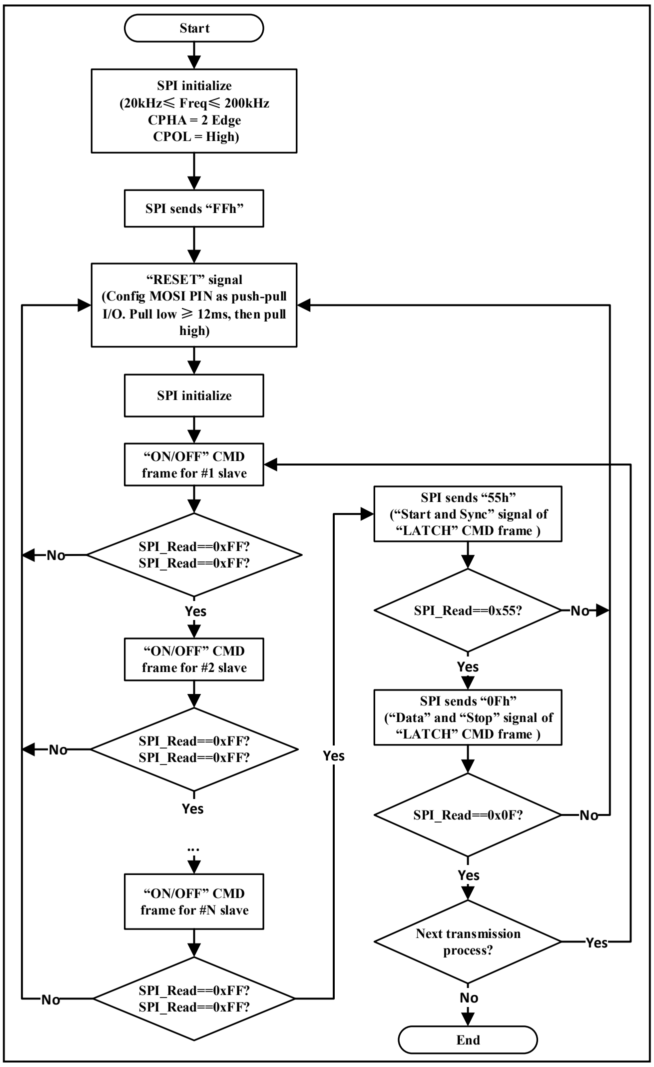



**Figure 44** Flowchart MISO Line Monitors DOUT

## ONEWIRE SERIAL BUS TIME-OUT

During the idle state (logic high), a low going pulse caused by EMI noise coupling may falsely start the command receiving of the device. The state machine will be stuck in "Start and Sync" signal receiving state and cannot successly receive the next valid command frame. To prevent that, a time-out timer is started on the low going pulse. Once the time-out period (9ms Typ.) expires, the state machine automatically exits from the "Start and Sync" signal receiving state and goes into the standby mode for command frame receiving.

## COMMUNICATION RELIABILITY

To mitigate the EMI noise interference, the copper traces of the onewire BUS cascaded connection on PCB board should be as short and thin as possile. It is recommended to surround them by ground plane.

Since the onewire serial BUS is asynchronous communication, the duty cycle ($D_{DIN}$) of $T_C$, which includes both of logic high and logic low, is critical for the communication success. It must be controlled within 35%~65%. Due to the propagation delay time asymmetry of signal rising edge and falling edge, the more devices cascaded, the greater duty cycle $D_{DIN}$ varies. When cascaded devices is up to 30, a lower data rate could be used to ensure the communication reliability. In order to improve EMI immunity, a noise decoupling capacitor might be considered to be added from each DIN pin to ground. However, the capacitor brings in more propagation delay time asymmetry. So a too large capacitor is not recommended. A 10pF capacitor is sufficient for most applications. This capacitor should be placed as close to the DIN pin as possible.

## FAULT PROTECTION AND REPORTING

For a robust system reliability, the IS32LT3141B integrates the detection circuitry to protect various fault conditions and report the fault conditions on the FAULTB pin which can be monitored by an external host. The fault protections include LED string open/short, output over-current (not reported) and thermal shutdown. The FAULTB pin is an open drain structure with an internal 50kΩ (Typ.) resistor pulled up to an internal 4.5V (Typ.) LDO so it is allowed to float. The FAULTB pin will go low when the device enables fault detection and detects a fault condition. Refer to Table 3.

The fault protection supports 'one fail all fail' mode, see Table 3; the FAULTB pin supports both input and output functions. Externally pulling FAULTB pin low will disable the output. For lighting systems with multiple IS32LT3141B drivers which requires the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection. A fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the "one fail all fail" operating requirement.

## LED STRING OPEN PROTECTION

The LED string open detection is enabled if the UV pin voltage is above its rising voltage threshold, $V_{UV\_IH}$, and disabled if below its falling voltage threshold, $V_{UV\_IL}$. A proper resistor divider ($R_{UV1}$ and $R_{UV2}$) connected from VIN pin to UV pin can set a UVLO function for LED string open protection, which is to prevent insufficient $V_{IN}$ falsely triggering LED string open detection. The UVLO voltage threshold is programmed by the resistor divider (Figure 45).

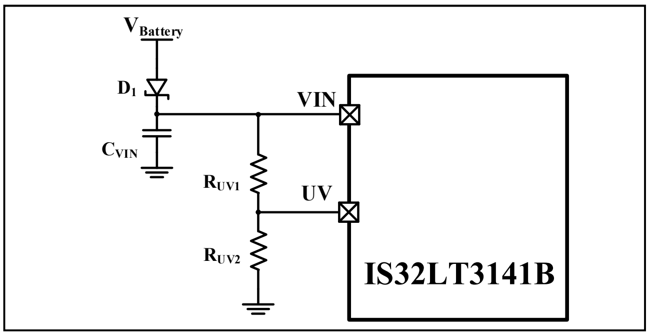



**Figure 45** UVLO for LED String Open Detection

$$V_{UVLO\_FLTF} = V_{UV\_IL} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \quad (3)$$

$$V_{UVLO\_FLTR} = V_{UV\_IH} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \quad (4)$$

It is recommend to set $V_{UVLO\_FLTF}$ at least 0.5V higher than the LED string voltage. Choose $R_{UV1}$ and $R_{UV2}$ to be 1% accuracy resistors with good temperature characteristic to ensure a stable and precise detection. On the PCB layout, this resistor divider must be placed as close to UV pin as possible to avoid noise interference. If the UV pin is unused, connect it to VIN pin via a resistor (recommended value is 10kΩ).

If the LED string is open, the OUT pin will be pulled up close to VICC pin voltage by the current source. If $V_{IN}$>$V_{UVLO\_FLTR}$ and the VICC pin to OUT pin voltage drop, ($V_{VICC}$-$V_{OUT}$), falls below the open LED detect voltage threshold, $V_{OD\_R}$, and persists for longer than the deglitch time $t_{FD\_DT}$, the LED string open protection will be triggered and FAULTB pin will go low to report the fault condition. The output source will reserve a small current $I_{RTR}$ for recovery detection.

The device will recover to normal operation and FAULTB pin will go back to high once the open condition is removed, ($V_{VICC}$-$V_{OUT}$) rising above the open LED detect voltage threshold, $V_{OD\_F}$.

## LED STRING SHORT PROTECTION

The LED string short condition is detected if the OUT pin voltage is lower than the short detect voltage threshold, $V_{SCD\_F}$. Once short condition occurs and persists for longer than the deglitch time $t_{FD\_DT}$, the LED string short protection will be triggered the FAULTB pin will go low to report the fault condition. The output source will reserve a small current $I_{RTR}$ for recovery detection.

The device will recover to normal operation and FAULTB pin will go back to high once the short condition is removed, OUT pin voltage rising above the short detect voltage threshold, $V_{SCD\_R}$.

## THERMAL SHUTDOWN

In the event that the junction temperature exceeds $T_{SD}$ (Typ. 175˚C), the output source will go to the "OFF" state and FAULTB pin will pull low to report the fault condition. At this point, the IC presumably begins to cool off. Any attempt to toggle the channel back to the source condition before the IC cooled to below ($T_{SD}$-$T_{HY}$) (Typ. 150˚C) will be blocked and the IC will not be allowed to restart. The FAULTB pin will recover to high once the IC has cooled down.

**Table 3 Fault Actions**

| UV Pin | Fault Type | Fault Condition | Output State | FAULTB Pin | Recovery |
|---|---|---|---|---|---|
| $<V_{UV\_IL}$ | LED string open or OUT short to VIN | Disabled | | | |
| | LED string short or OUT short to GND | $V_{OUT}<V_{SCD\_F}$ | Outputs $I_{RTR}$ for recovery detection | Pull low (If the FAULB pins of multiple devices are connected together, all devices will be off) | $V_{OUT}>V_{SCD\_R}$ |
| | Over temperature | $T_J>T_{SD}$ | Off | | $T_J<(T_{SD}-T_{HY})$ |
| $>V_{UV\_IH}$ | LED string open or OUT short to VIN | $(V_{VICC}-V_{OUT})<V_{OD\_R}$ | Outputs $I_{RTR}$ for recovery detection | | $(V_{VICC}-V_{OUT})>V_{OD\_F}$ |
| | LED string short or OUT short to GND | $V_{OUT}<V_{SCD\_F}$ | Outputs $I_{RTR}$ for recovery detection | | $V_{OUT}>V_{SCD\_R}$ |
| | Over temperature | $T_J>T_{SD}$ | Off | | $T_J<(T_{SD}-T_{HY})$ |

## THERMAL CONSIDERATIONS

The package thermal resistance, $\theta_{JA}$, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The $\theta_{JA}$ is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, $T_J$, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3141B, $P_{3141B}$, and the package thermal resistance, $\theta_{JA}$, as in Equation (5):

$$T_J = T_A + \Delta T = T_A + P_{3141B} \times \theta_{JA} \quad (5)$$

When operating the chip at high ambient temperatures, or when the supply voltage is high, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation at $T_A$=25˚C can be calculated using the following Equation (6):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \quad (6)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{43.6°C/W} \approx 2.87W \quad (7)$$

for SOP-8-EP package.

Figure 46, shows the power derating of the IS32LT3141B on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

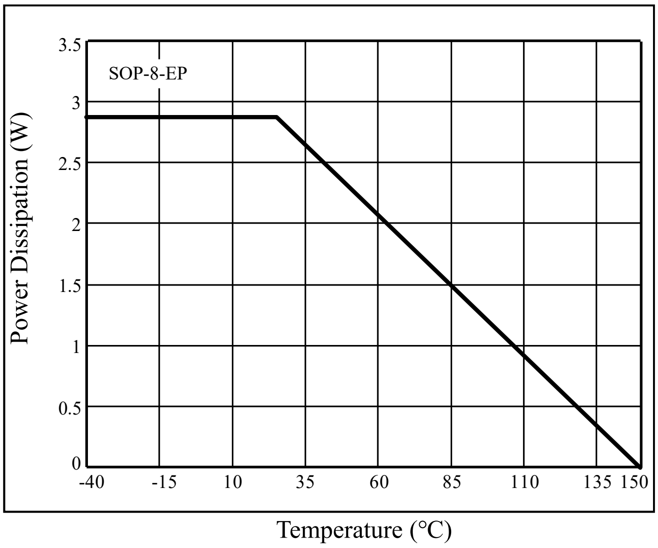



**Figure 46** Dissipation Curve (SOP-8-EP)

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a large copper area on each side of the board directly under the IS32LT3141B. Multiple thermal vias, as shown in Figure 47, will help to conduct heat from the exposed pad of the IS32LT3141B to the copper on each side of the board.

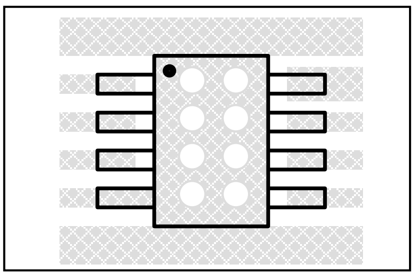


**Figure 47** Board Via Layout For Thermal Dissipation

### CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|---|
| **Preheat & Soak**<br>Temperature min (Tsmin)<br>Temperature max (Tsmax)<br>Time (Tsmin to Tsmax) (ts) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3°C/second max. |
| Liquidous temperature (TL)<br>Time at liquidous (tL) | 217°C<br>60-150 seconds |
| Peak package body temperature (Tp)* | Max 260°C |
| Time (tp)** within 5°C of the specified classification temperature (Tc) | Max 30 seconds |
| Average ramp-down rate (Tp to Tsmax) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

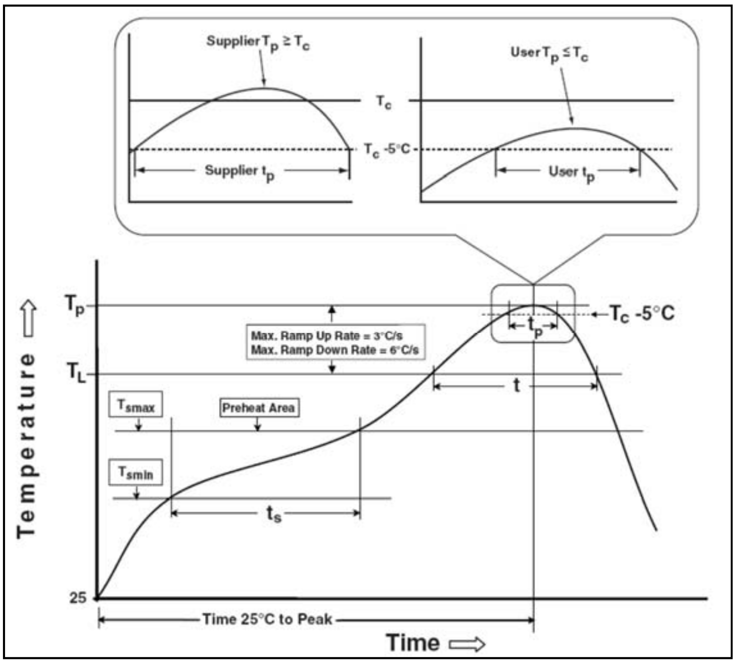
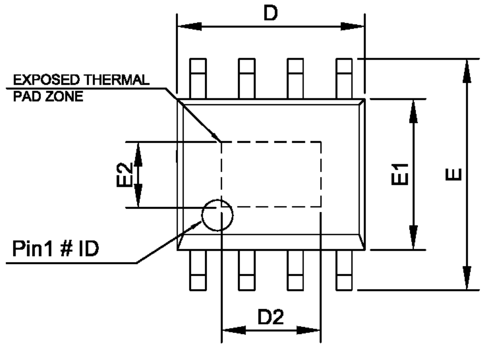
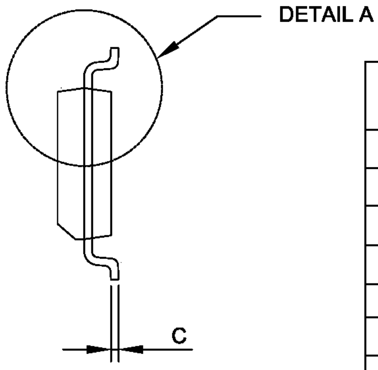


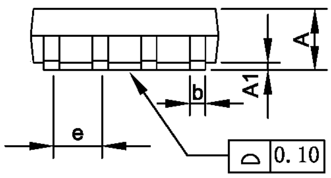

**Figure 48** Classification Profile

## PACKAGE INFORMATION

### SOP-8-EP

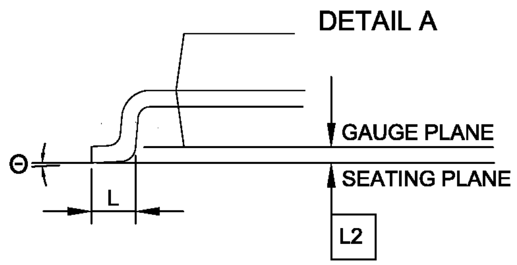



| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | – | – | 1.70 |
| A1 | – | – | 0.15 |
| E1 | 3.70 | 3.90 | 4.10 |
| E | 5.80 | 6.00 | 6.20 |
| D | 4.70 | 4.90 | 5.10 |
| b | 0.31 | – | 0.51 |
| e | 1.27BSC | | |
| L | 0.40 | – | 1.27 |
| L2 | 0.25BSC | | |
| θ | 0° | – | 8° |
| C | 0.10 | – | 0.25 |
| D2 | 1.50 | – | – |
| E2 | 1.00 | – | – |

233-570-289 Rev. B

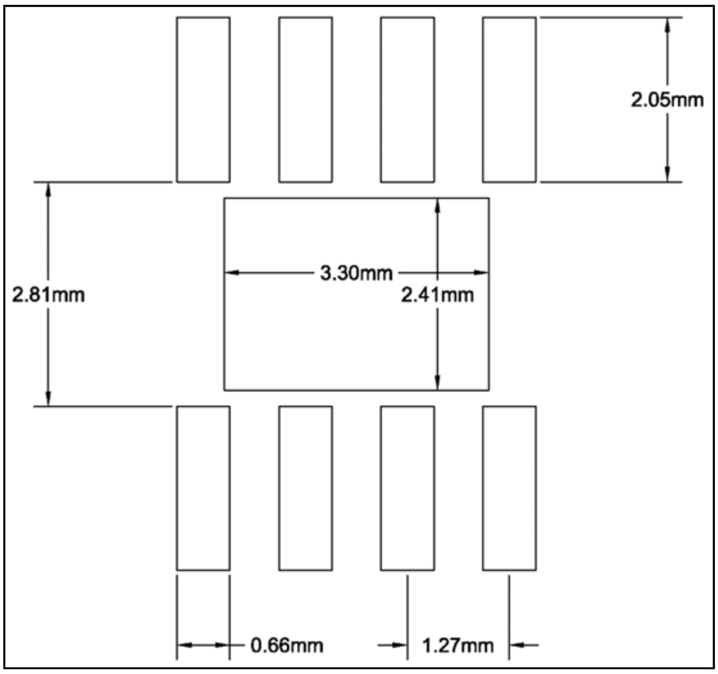



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY AND THERMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

## RECOMMENDED LAND PATTERN

### SOP-8-EP




**Note:**

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

## REVISION HISTORY

| Revision | Detail Information | Date |
|---|---|---|
| 0A | Initial release | 2021.09.16 |
| A | Udpate to final version | 2021.12.27 |